2024 차세대 리소그래피 + 패터닝 학술대회

ABSTRACT BOOK

Pioneering the Future :

Charting New Directions in Lithography and Patterning

AUG. 12 (MON) - 13 (TUE), 2024

Suwon Convention Center, SUWON | 수원 컨벤션 센터

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Invitation 초대의 글

Welcome to the 2024 Next Generation Lithography + Patterning Conference!

Dear Colleagues,

We are delighted to extend our invitation to the 2024 Next Generation Lithography + Patterning Conference, scheduled to take place at the Suwon Convention Center from August 12th (Mon.) to 13th (Tue).

As the semiconductor industry continues to evolve and innovate, lithography and patterning technologies remain at the forefront of these advancements. This year's conference promises to be an invaluable opportunity for industry leaders, researchers, and academics to convene and exchange insights on the latest developments in these critical areas.

Building upon the success of previous years, we have expanded our program to include a new session on 'Advanced Etch Technology for Nanopatterning,' reflecting the growing importance of this field in semiconductor fabrication.

In addition to our plenary/keynote talks and technical/panel-discussion sessions, attendees can look forward to engaging poster presentations, networking opportunities, and interactions with industry partners and vendors. We believe that these interactions will foster collaboration, inspire innovation, and drive the continued progress of the semiconductor industry.

Once again, the Suwon Convention Center will serve as our venue, offering a convenient and conducive environment for meaningful discussions and networking. Situated adjacent to the scenic Gwanggyo Lake Park and surrounded by Suwon's iconic landmarks, the venue provides the perfect backdrop for our conference.

We eagerly anticipate your participation in this year's event as we collectively shape the future of lithography and patterning technologies through collaboration and ingenuity.

Warm regards,

2024 Conference Organizing Committee Chair Jong-Rak Park, Jinho Ahn
Program Committee Chair Byoung-Ho Lee, Jun Ho Lee

Organizing Committee Chair

Jong-Rak Park
Professor
Chosun University

Jinho Ahn
Professor
Hanyang University

Program Committee Chair

Byoung-Ho Lee
Fellow
Hitachi Hightech

Jun Ho Lee
Professor
Kongju National University

Committee 학술대회 위원회

조직위원회

조직위원회 위원 명단

(총괄) 위원장 : 박종락(조선대), 안진호(한양대)

(소위원회) (가나다순)

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재무위원회	위원장	차병철(Entegris)
	위원	여정호(AMAT), 이병규(삼성전자), 이혁교(KRISS), 정용철(KITECH), 최준혁(KIMM)
출판위원회	위원장	이대호(가천대)
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논문상심사위원회	위원장	김성환(한양대)
	위원	이상설(포항공대 가속기연구소), 이준호(공주대), 이진균(인하대)
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	위원	강경태(KITECH), 김성수(서울대), 김재순(명지대), 백기호(D2S), 송윤호(피코팩), 안승준(선문대), 오혜근(한양대), 유우식(WaferMasters), 이승걸(인하대), 조한구(FST), 한재원(연세대)

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프로그램위원회 위원 명단

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(분과위원회) (가나다순)

Optical and EUV Lithography	위원장	이상설(포항공대 가속기연구소)
	위원	강영석(삼성전자), 김건수(LG전자), 김병국(이솔), 김성수(서울대), 김후식(뷰웍스), 남정림(한양대), 문성용(FST), 박동운(SEMES), 박종락(조선대), 승병훈(S&S TECH), 안진호(한양대), 여정호(AMAT), 이윤우(KRISS), 이혁교(KRISS), 임창문(SK hynix), 전영민(KIST), 정수화(LG전자), 최성운(HIMS), 최성원(FST), 최정동(TechInsights), 최진(삼성전자), 한재원(연세대), 황찬(삼성전자)
Patterning Materials and Processes	위원장	이진균(인하대), 허수미(전남대)
	위원	고차원(삼성전자), 김명웅(인하대), 김현우(삼성전자), 복철규(동진세미켐), 여기성(JSR), 우상균(SEMES), 유정윤(Versum Materials), 임재봉(DuPont), 장지현(UNIST), 전성호(LG화학), 정진항(ASML), 정현담(전남대), 차병철(Entegris)
Alternative Lithography and Nano Fabrication	위원장	이승우(고려대), 전석우(고려대)
	위원	강경태(KITECH), 김대근(단국대), 김명기(고려대), 김선경(경희대), 김성환(한양대), 노준석(포항공대), 이대호(가천대), 이병규(삼성전자), 정건영(GIST), 정연식(KAIST), 정용철(KITECH), 최준혁(KITECH)
Computational Lithography	위원장	양현조(ASML)
	위원	고성우(SK hynix), 김령한(IMEC), 서정훈(ASML), 신영수(KAIST), 안창남(Siemens EDA), 양승훈(삼성전자), 오혜근(한양대), 이승걸(인하대), 최병일(Synopsys)
Metrology and Inspection	위원장	이명준(삼성전자)
	위원	김대석(전북대), 김두리(한양대), 김영식(KRISS), 김욱래(삼성전자), 김재완(KRISS), 김태곤(한양대), 김향균(홍익대), 류성윤(삼성전자), 마성민(SK hynix), 박병천(KRISS), 안희경(KRISS), 이성우(Carl-Zeiss), 이성은(삼성전자), 이종규(미래로시스템), 임선종(KIMM), 장무석(KAIST), 전병환(인하대), 조태영(삼성전자), 주기남(조선대), 진종한(KRISS)
Dry Etch	위원장	정진욱(한양대)
	위원	권광호(고려대), 김동찬(ASML Brian), 김무성(Gauss Lab), 김용진(SK hynix), 김윤재(삼성전자), 민경진(명지대), 박종철(삼성전자), 배근희(삼성전자),서희찬(SK hynix), 양장규(삼성전자), 염근영(성균관대), 유신재(충남대), 임연호(전북대), 조성일(삼성전자), 한영훈(SK hynix), 홍상진(명지대)

Detailed Schedule

Detailed Schedule 학술대회 세부일정

1st Day | Aug. 12, 2024 (Mon.)

08:00-09:00	Registration		
09:00-10:25	PL-I Plenary Session [405-408] Chair: 김용진 (SK hynix)		
	Opening Remarks | 프로그램위원장 개회사, 이병호 (히타치하이테크) Plenary Talk 1 | Plasma sources in the semiconductor processing : What has been used and what will be necessary, 배근희 (삼성전자) Plenary Talk 2 | Lithography, Metrology, and Inspection in the Age of Accelerator Light Sources, Erik R. Hosler (FylEx and xLight)		
10:25-10:45	Break		
10:45-12:15	EU-I [401/402] **EUV Lithography I** Chair: 이상설 (포스텍)	MI-I [405/406] **Advanced Metrology and Inspection I** Chair: 이명준 (삼성전자)	
	EU-I-1(초청) 민철기 (삼성전자) EU-I-2(초청) 이동근 (ESOL) EU-I-3(초청) 김동언 (포스텍)	MI-I-1(초청) 한상현 (NOVA) MI-I-2(초청) 정재훈 (삼성전자) MI-I-3(초청) 장무석 (KAIST)	
12:15-13:30	Lunch/Break		
13:30-15:00	EU-II [401/402] **EUV Lithography II** Chair: 김병국 (ESOL)	MI-II [405/406] **Advanced Metrology and Inspection II** Chair: 김욱래 (삼성전자)	ET-I [403] **Advanced Etch Technology for Nanopatterning I** Chair: 민경진 (명지대)
	EU-II-1(초청) 김황범 (SK hynix) EU-II-2(초청) 승병훈 (S&S TECH) EU-II-3(초청) 김형준 (한국세라믹기술원)	MI-II-1(초청) Sean Park (KLA) MI-II-2(초청) 장혜진 (서울대) MI-II-3(초청) Eugen Foca (Zeiss)	ET-I-1(초청) 이재원 (SK hynix) ET-I-2(초청) 임연호 (전북대) ET-I-3(초청) 정진욱 (한양대)
15:00-15:20	Break		
15:20-16:50	PL-II Plenary Session II [405-408] Chair: 이명준 (삼성전자)		
	Welcome Remarks | 조직위원장 환영사, 안진호 (한양대) | 한국광학회 (차기)회장 축사, 이상민 (KAIST) Plenary Talk 3 | Exploring the Past, Present, and Future of Metrology and Inspection Technologies in Semiconductor Manufacturing Processes: Perspectives on Fundamentals, Challenges, and Expansion, 양유신 (삼성전자) Plenary Talk 4 | Extension of memory devices and technology direction of photo lithography, 서재욱 (SK hynix)		
16:50-17:10	Break		
17:10-18:30	Panel Discussion [405-408] Chair: 이상설 (포스텍)		
	| 주제 | **"Scale down (EUV HNA Challenges) + 3D Architecture"** | 패널 | 고차원 (연세대), 김재현 (SK hynix), 양유신 (삼성전자), 배근희 (삼성전자), 서재욱 (SK hynix), 최리노 (인하대)		
18:30-20:30	**Banquet : 마키노차야 광교점** | 진행 | 남정림 (한양대)		

Detailed Schedule 학술대회 세부일정

2nd Day | Aug. 13, 2024 (Tue.)

08:00-09:00	Registration		
09:00-10:30	PS Poster Session [4th Floor Lobby]		
10:30-12:00	PL-III Plenary Session III [405-408] Chair: 허성민 (ASML)		
	Appreciation Remarks | 프로그램위원장 감사의 말씀, 이준호 (공주대) Plenary Talk 5 | Backside patterning from lithography perspective: alignment, metrology, and overlay control, 성낙근 (ASML) Keynote Talk 1 | Navigating the Road to Silicon Valley, Simon Lee (KASASV)		
12:00-13:30	Lunch/Break		
13:30-15:00	PM-I [401/402] **Patterning Materials I** Chair: 허수미 (전남대)	LO-I [405/406] **Layout Optimization and Computational Lithography I** Chair: 양현조 (ASML)	AL-I [403] **Alternative Lithography I** Chair: 김명기 (고려대)
	PM-I-1(초청) 정현담 (전남대) PM-I-2(초청) 서용범 (삼성전자) PM-I-3 구예진 (인하대) PM-I-4 윤세현 (전남대)	LO-I-1(초청) 김은주 (삼성전자) LO-I-2(초청) 김성호 (SK hynix) LO-I-3(초청) 송정철 (National NanoFab)	AL-I-1(초청) 심태섭 (아주대) AL-I-2(초청) 강문성 (서강대) AL-I-3(초청) 정현호 (GIST)
15:00-15:20	Break		
15:20-16:50	PM-II [401/402] **Patterning Materials II** Chair: 고차원 (연세대)	LO-II [405/406] **Layout Optimization and Computational Lithography II** Chair: 양현조 (ASML)	AL-II [403] **Alternative Lithography II** Chair: 김명기 (고려대)
	PM-II-1(초청) 윤효재 (고려대) PM-II-2(초청) 이진균 (인하대) PM-II-3 김현석 (전남대)	LO-II-1(초청) Ulrich Welling (Synopsys) (Online)	AL-II-1(초청) 노유신 (건국대) AL-II-2(초청) 한상윤 (DGIST) AL-II-3(초청) 김인기 (성균관대)
16:50-17:10	Break		
17:10-17:30	CL Closing Session [405/406] Chair: 김성환 (한양대)		
	Best Student Paper Awards Ceremony | 학생논문상 심사평, 김성환 (한양대) | 학생논문상 시상, 정진항 (ASML) Closing Remarks | 조직위원장 폐회사, 박종락 (조선대)		

Plenary Talks

Plenary Talk 1

Plasma sources in the semiconductor processing : What has been used and what will be necessary

배근희
| Master, 삼성전자

Abstract

Plasma has been widely used in the semiconductor processing for decades due to its many proper properties for processing. Plasma makes processing fast and enhances vertical profiles. Additionally, plasma processing enables low temperature process which is crucial for decreasing heat budget to the semiconductor devices, and improves the particle problems falling to the wafers. For these reasons the plasma has expanded its regime in the semiconductor processing to all the area of processing. Due to its key role in the process, there have been many researches to find the most suitable plasma for each process. For example, there were many researches to adapt the high density plasma sources like ICP or helicon to the oxide etching, but most of them failed and there were least trials of that these days. Instead, other researches for various kinds of pulsing have been successful and are widely used in the business. In this presentation I will review the history and the current status of the plasma processing in the semiconductor business and wish to discuss what will be necessary in the future in the plasma processing

Biography

Dr. Bai is a V.P. of tech (Master) in Samsung semiconductor R&D center. He has worked with responsibility on developing patterning since 2002. Recently he is leading EUV patterning in the R&D center. He received a Ph.D degree in plasma physics from KAIST, Daejeon, Korea. His Ph.D thesis was controlling the plasma parameter using a biased grid and gas mixing. He has published more than 50 papers and patents on his research area.

Lithography, Metrology, and Inspection in the Age of Accelerator Light Sources

Erik R. Hosler
| Founder, FylEx and xLight

Abstract

Light is the critical driver for leading-edge semiconductor manufacturing. The properties, quality, and quantity of light at specific wavelengths determines the manufacturable device performance and economics.
Therefore, innovations in light source technology fuel our modern economy. Photolithography is the quintessential innovation cycle between light source and manufacturable transistor; however, this trend is now evolving more rapidly in metrology and inspection as device critical features approach near atomic dimensions, architectures evolve to three dimensional geometries, and cycle time between nodes and products must keep pace.

Particle accelerators offer the means to construct multifaceted, utility-scale light sources with unprecedent manufacturing capability that can dramatically reshape the economics beyond the semiconductor industry. Cost and capability scaling of lithography driven by a free - electron laser would drastically alter the economics of Moore's Law as we know it, and the advances in wavelength, resolution, sensitivity, and throughput in metrology and inspection applications would similarly reshape the research, development, and process control strategies. The paradigm shift of accelerator-based light sources will be the most dramatic shift in semiconductor manufacturing history, and the reverberations will affect both parallel and tangential industries.

Biography

Erik Hosler has founded several companies, including FylEx and xLight, organizations focused on industrializing particle accelerator technology and the associated applications to deliver a paradigm shifting light source technology for semiconductor manufacturing and beyond. Erik received his PhD from the University of California, Berkeley in Physical Chemistry, and afterwards he went into lithography research and development at GlobalFoundries, eventually leading the industrialization program of EUV lithography. He has published a variety of technical papers on lithography and light source technology, including on industrialized free-electron lasers. Erik also worked at PsiQuantum as the lithography and patterning strategist for initial silicon photonic quantum computing test vehicles before starting xLight and FylEx to drive the industrialization of novel light source architectures.

Plenary Talk 3

Exploring the Past, Present, and Future of Metrology and Inspection Technologies in Semiconductor Manufacturing Processes
: Perspectives on Fundamentals, Challenges, and Expansion

양유신
I Fellow, 삼성전자

Abstract

In the rapidly evolving field of semiconductor devices, significant technological milestones have been achieved for DRAM, Flash, and Logic devices. This talk will provide a historical overview of these developments, tracing their technological advancements and examining the metrology and inspection (MI) technique, one of the key technologies that enabled such advancements. Furthermore, we will also examine the current challenging MI issues related to semiconductor devices and the recently introduced advanced packaging (AVP) process. One of the goals of this talk is to provide a comprehensive overview of the various challenges encountered and explore potential solutions to address these issues, particularly from the perspectives of detecting nano-sized pattern defects and measuring nanostructures. This will involve a detailed analysis of the current state-of-the-art MI technologies, as well as an evaluation of the potential benefits and limitations of recently emerging AI-based approaches for addressing these challenges. A comprehensive view of the developmental trajectory of MI technologies, covering its fundamentals, challenges, and future expansion will be covered in the talk in detail.

Biography

Yusin Yang, is Fellow and has been working in SAMSUNG Electronics CO. since 2000. He received B.S. and M.S. in Physics at KAIST(Korea Advanced Institute of Science and Technology) in 1993 and 1995. And in 2000, he received his Ph.D. from KAIST with a dissertation on crystal growth and characterization of KTiOPO4(KTP) isomorphs.

Since joining Samsung Electronics CO. in 2000, he has worked on developing MI (Metrology and Inspection) technology for memory semiconductor device by 2019 and has expanded his work into logic device since 2020. Now he is responsible for establishing MI technology strategy for the entire semiconductor devices after being appointed as company Fellow in 2022.

His research focuses on in-line MI technology to detect nano-size defects and measure sub-nano-size patterns structures especially for the next-generation semiconductor devices. The technology includes various microscopic areas from optical to electron microscope expanding applicable spectral range. In optical microscope his study has been focusing on developing the contrast enhancement technology for the virtual resolution enhancement. In electron microscope he is developing multi-beam technology to overcome the disadvantage of electron beam scan speed. In order to measure subsurface nano-size structures, conventionally SE(Spectroscopic Ellipsometry) and high voltage SEM(Scanning Electron Microscope) technologies are used. For more development of those technologies he is studying advanced RCWA(Rigorous Coupled Wave Analysis) method with AI(Artificial Intelligence) algorithms. As a future application using SEM technology, his study includes three-dimensional SEM concept development.

He has more than 140 patents and has authored or coauthored several papers in the field of semiconductor MI technology. For the future, he is trying to develop innovative MI methodology which can be the potential for the next generation 3D semiconductor devices.

Extension of memory devices and technology direction of photo lithography

서재욱
| Vice President, SK hynix

Abstract

The extension of the 2D baseline platform in DRAM devices is facing challenges caused by the limitation of patterning and device performance. The adoption of new lithography technologies for Stack-Up structures in NAND devices are being necessitated due to the evolving patterning process. Especially, In the DRAM devices, the on-going development of various lithography technologies aims to decrease CapEX and OpEX for Extreme Ultraviolet (EUV). Moreover, it is crucial to define and prepare lithography technologies that incorporate advanced concepts in alignment with the shift towards new technological platforms such as VG or 3D-DRAM. In order to thrive in this industry within a continuously evolving ecosystem, it is imperative to develop photo process technologies that prioritize maximizing the EUV applications including High-NA EUV, advancing OPC (Optical Proximity Correction) technologies, optimizing patterning process through advanced metrology analysis methods based on Big-Data and creating breakthrough technologies to address the limitations of overlay correction capabilities. Moreover, establishing an assertive collaboration model with business partners and innovating the methodologies within R&D are essential in developing equipment with newly introduced concepts. This lecture will explore the challenges and future directions of photolithography technologies, based on insights from the industrial perspective within the memory market sector, considering key aspects of the technological roadmap.

Biography

Jaewook Seo is the vice president of R&D photo process department at SK hynix. He received B.S. in ceramic engineering from Yonsei University in 1998. After joining SK hynix in 1998, he participated in the development of DRAM photo process for various generations of tech. node. He was appointed as vice president of R&D photo process in 2022 after serving as the head of the advanced photo team in 2019.

Currently, he is in charge of research and development of photolithography roadmap for DRAM, NAND, and new memory devices. His research focuses on developing new patterning technologies in preparation for the transition of DRAM to new platforms such as VG/3DDRAM and overcoming the limitations of DRAM/NAND patterning. He is also in charge of developing advanced OPC technologies such as High-NA EUV OPC and ML based OPC applications from 2023.

Backside patterning from lithography perspective : alignment, metrology, and overlay control

성낙근
| Director of TDC US/Asia of ASML, ASML

Abstract

Lithography resolution has been driving dimensional scaling of semiconductor devices, but nowadays it is more and more complemented with device level 3D architectures (such as Gate-all-around) and system level 3D integration (such as stacked SRAM on Logic and 3D DRAM on Memory). Logic backside power delivery network (BS-PDN) is a disruptive innovation that offers significant performance gain in combination with higher transistor density. Key feature of this technology is the ability to connect to the already fully processed front-end devices from the backside. This connection takes place after fusion bonding and requires, depending on the chosen process flow, a single digit tight post-bonding scanner overlay control.
In this presentation, we will discuss implications of the BS-PDN processing on scanner alignment, overlay metrology, and overlay control for the post-bonding exposures. We will show that a significant improvement is possible to meet the overlay performance requirement by applying high order corrections per exposure of the scanner and we will discuss additional opportunities to improve the performance. We will pay special attention to the wafer edge (R > 135mm) as in this region it will be most challenging to achieve the required post-bonding overlay

Biography

Nak Seong is Director of TDC US/Asia of ASML. He joined ASML TDC, Technology Development Center, in November 2013. His work covers studies of future semiconductor technology trends to understand requirements of future patterning technologies. From 2007 to 2013, he worked at Cymer guiding product developments and driving customer interactions by analyzing patterning impact of light sources. From 2001 to 2006, he worked at IBM where he worked on high NA imaging, 157 lithography development, and DFM for low k1 imaging. He started his career at Samsung in Korea in 1989 where he developed lithography processes for DRAM in early days, and developed RET for low k1 imaging solutions for memory products and scanner evaluation methods to support them. He graduated Kyung-Hee university in 1989 with BS in Physics.

Plenary Talks

Navigating the Road to Silicon Valley

Simon Lee
| Founder/Executive, KASASV

Abstract

Embarking on a career journey towards Silicon Valley is like setting off on an adventure into the heart of innovation and opportunity. In this keynote, we'll break down what Silicon Valley is all about, focusing on its semiconductor industry and the exciting world of artificial intelligence. We'll cover everything from the history and main players to the unique culture that sets this place apart.

We'll dive into the corporate world of semiconductor giants and explore the various career paths available, whether it's sales, marketing, engineering, or something else. And we'll stress the importance of networking, showing how making connections can really boost your career prospects.

Drawing on my own experiences over the past twenty-eight years, working at companies like SVG, ASML, Therma-Wave, Integrated Materials, and KLA, we'll look at how I got to Silicon Valley and what I learned along the way. We'll talk about key moments like company acquisitions and moving internationally, and I'll share some tips for navigating these challenges.

But here's the thing: there's no magic formula for success in Silicon Valley. It takes hard work and planning. So, I'll encourage you to start thinking about your future now - not just in vague terms, but with specific goals for where you want to be in one year, two years, five years, and beyond.

And remember, networking is key - both in Silicon Valley and wherever else your career may take you.

So, join me as we embark on this journey to Silicon Valley, where every challenge is an opportunity and every connection can make a difference.

Biography

Simon Lee is the Chairman of KASASV(Korean American Semiconductor Silicon Valley), non-profit organization in Silicon Valley. He is a seasoned professional with over twenty years of experience in the global semiconductor industry, specializing in sales, business development, and strategic leadership. His career in Semiconductor Equipment Industry started from SVG, ASML, Thermawave, Integrated Materials, and KLA and led Corporate Sales from HQ to Korea region as well as Worldwide region depending upon roles at each company and has broad range of semiconductor process equipment experiences from Photo, Litho, Diffusion, APCVD, Metrology and Inspections. He holds MS in MIS and MA in Computer Education from USIU (a.k.a. Alliant Int'l University).

Panel Discussion

Panel Discussion

●●● Agenda

“Scale down (EUV HNA Challenges) + 3D Architecture”

2024년 8월 12일(월) 17:10~18:30 수원컨벤션센터 405-408호

- 좌 장 : 이상설 (포스텍)
- 패 널 : 고차원 (연세대), 김재현 (SK hynix), 양유신 (삼성전자), 배근희 (삼성전자), 서재욱 (SK hynix), 최리노 (인하대)

시 간	프로그램	내용
17:10	개회	개회 및 패널 소개
17:12	발제발표	차원 반도체의 시대: 지속 가능한 신 무어의 법칙으로 가는 길은 무엇인가?
17:15	주제발표	3D 반도체 시대의 리소그래피에 대한 6인 전문가의 한 줄 평가
17:30	지정토론	| 3차원 반도체 시대, 리소그래피의 미래와 반도체 산업의 방향 | 초미세화 도전 과제, High-NA EUV 시대의 리소그래피 재료, 공정 기술의 과제 | 무어의 법칙 한계를 극복할 새로운 기술 대응 방향 | 미래의 반도체人, 학생들에게 보내는 선배들의 한마디
18:00	자유토론	청중 질의 및 패널 답변
18:30	폐　회	정리 및 폐회

Oral Presentation Session

Oral Presentation Session

EU-I	EUV Lithography I	10:45-12:15. August 12 (Mon), 2024 [Room 401-402] 좌장 : 이상설(포스텍)
EU-I-1 Invited	EUV Mask Inspection Technologies for DRAM and Logic EUV Lithography *<u>민철기</u> (삼성전자)	
EU-I-2 Invited	Development Of High-Brightness Xe LPP Source And Its Application *<u>이동근</u> (ESOL)	
EU-I-3 Invited	Next-generation science and technology in EUV source *<u>김동언</u> (포스텍)	

EU-II	EUV Lithography II	13:30-15:00. August 12 (Mon), 2024 [Room 401-402] 좌장 : 김병국 (ESOL)
EU-II-1 Invited	High-NA EUV lithography and its challenge on depth of focus *<u>김황범</u> (SK hynix)	
EU-II-2 Invited	Challenges of EUV Blankmask Technology in High NA EUV Lithography *<u>승병훈</u> (S&S TECH)	
EU-II-3 Invited	EUV 포토마스크용 LTEM 소재 *<u>김형준</u> (한국세라믹기술원, KICET)	

MI-I	Advanced Metrology and Inspection I	10:45-12:15. August 12 (Mon), 2024 [Room 405-406] 좌장 : 이명준 (삼성전자)
MI-I-1 Invited	Advanced Metrology Journey for Future Device Challenges *<u>한상현</u> (NOVA)	
MI-I-2 Invited	Simulation-based MI and Digital Twin Technology for Semicoductor *<u>정재훈</u> (삼성전자)	
MI-I-3 Invited	Exploring Generalization Capability of Deep Learning-Based Approaches for Holographic Image Reconstruction: Opportunities in Semiconductor Metrology & Inspection *<u>장무석</u> (KAIST)	

MI-II	Advanced Metrology and Inspection II	13:30-15:00. August 12 (Mon), 2024 [Room 405-406] 좌장 : 김욱래 (삼성전자)
MI-II-1 Invited	Broadband Plasma Inspection Technology and Semiconductor High-Volume Manufacturing *<u>Sean Park</u> (KLA)	
MI-II-2 Invited	Multiscale Thermal Metrology Bridging Nanoscale to Device Scale for Semiconductor Inspection *<u>장혜진</u> (서울대)	
MI-II-3 Invited	3D Tomography for semiconductor device manufacturing : the art of transforming an academic curiosity into an advanced metrology and inspection technique. *<u>Eugen Foca</u> (Zeiss)	

Oral Presentation Session

ET-I	Advanced Etch Technology for Nanopatterning I	13:30-15:00. August 12 (Mon), 2024 [Room 403] 좌장 : 민경진 (명지대)
ET-I-1 Invited	Hard mask pattern processing for high aspect ratio contact etch **이재원 (SK hynix)*	
ET-I-2 Invited	A realistic 3D topography simulation platform for addressing emerging issues **임연호 (전북대)*	
ET-I-3 Invited	Novel plasma sources for atomic scale etching **정진욱 (한양대)*	

PM-I	Patterning Materials I	13:30~15:00. August 13 (Tue), 2024 [Room 403] 좌장 : 허수미 (전남대)
PM-I-1 Invited	Leveraging the strenghths of cyclic siloxane molecules and overcoming its weakness through the invention of a novel cyclic stannoxane molecule for EUV inorganic resist **정현담 (전남대)*	
PM-I-2 Invited	W-curve method to define photoresist resolution in EUV lithography **서용범 (삼성전자)*	
PM-I-3	Radical-driven Sensitivity Improvement of Tin-oxo Clusters for High NA extreme UV Lithography **구예진 (인하대)*	
PM-I-4	Advancing High-Resolution VIA Pattern through DSA and EUVL Integration **윤세현 (전남대)*	

PM-II	Patterning Materials II	15:20-16:50. August 13 (Tue), 2024 [Room 401-402] 좌장 : 고차원 (연세대)
PM-II-1 Invited	Multinuclear Tin-based Macrocyclic Organometallic Resist for EUV Photolithography **유효재 (고려대)*	
PM-II-2 Invited	Sensitivity Enhancement of EUV Lithographic Patterning Using Tin-Containing Underlayer Materials **이진균 (인하대)*	
PM-II-3	Simulation Approaches for Exploring Process Conditions and Materials in EUV Lithography **김현석 (전남대)*	

LO-I	Layout Optimization and Computational Lithography I	13:30-15:00. August 13 (Tue), 2024 [Room 405-406] 좌장 : 양현조 (ASML)
LO-I-1 Invited	Rigorous 3D Probabilistic Computational Lithography and Chip Level Inspection for EUV Stochastic Failure Detection **김은주 (삼성전자)*	
LO-I-2 Invited	Expansion of Machine Learning Solution in OPC **김성호 (SK hynix)*	
LO-I-3 Invited	300mm size Wire grid polarizer(WGP) manufacturing method using 50nm line pattern stitching process technology in ArF immersion **송정철 (National NanoFab)*	

Oral Presentation Session

LO-II	Layout Optimization and Computational Lithography II	15:20-16:50. August 13(Tue), 2024 [Room 405-406] 좌장 : 양현조(ASML)
LO-II-1 Invited (Online)	Computational Lithography of Metal-Oxo-Resists *Ulrich Klostermann (Synopsys)*	

AL-I	Alternative Lithography I	13:30-15:00. August 13(Tue), 2024 [Room 403] 좌장 : 김명기 (고려대)
AL-I-1 Invited	Fabrication of mechanochromic structural color film through melt-shear assembly of a core-shell nanoparticles *심태섭 (아주대)*	
AL-I-2 Invited	Direct and Indirect Photolithography of Quantum Dots *강문성 (서강대)*	
AL-I-3 Invited	Shadow growth for plasmonics *정현호 (GIST)*	

AL-II	Alternative Lithography II	15:20-16:50. August 13(Tue), 2024 [Room 403] 좌장 : 김명기 (고려대)
AL-II-1 Invited	III-V/Si light source integration from on-demand to three-dimensional dimensions *노유신 (건국대)*	
AL-II-2 Invited	Co-integration of zero-static-power nanomachines with silicon photonics *한상윤 (DGIST)*	
AL-II-3 Invited	Advanced Nanofabrications for Nanophotonics: 3D EBL, Single-digit Nanometer Scale EBL and scalable NIL *김인기 (성균관대)*	

EU-I-1 (Invited) 10:45~11:15

EUV Mask Inspection Technologies for DRAM and Logic EUV Lithography

*민철기 (삼성전자)

As the design rule continues to shrink towards the EUV lithography and beyond, the EUV mask inspection is one of the most important technologies for HVM lithography. While studies on EUV inspection algorithm was mainly focused on masks for logic devices, we studied the EUV mask inspection technology for DRAM and LOGIC devices. In this paper, we will introduce EUV mask inspection technologies using DUV, Ebeam, and actinic tools. Especially, we will focus on curvilinear mask inspection and high-NA APMI development status for next-generation EUV lithography. First, the new technologies of DUV mask inspection will introduce using hybrid inspection for DB + DD integration and deep-learning based DB modeling. Second, the multi-columnrn based EBMI will introduce to realize higher sensitivity resolution, and throughput. Third, the APMI will introduce and investigate machine-learning based DB inspection algorithm to overcome resolution limit and accuracy of conventional DB modeling based DUV mask inspection. Finally, the new inspection technologies will introduce for next-generation EUV lithography (1) new optics and evaluation results to meet the requirements of 4X & 8Y anamorphic mask (2) new data format as multigonrnfor curvilinear EUV mask with SRAFs.

| Keywords : EUV Lithography, EUV Mask Inspection, EBMI, APMI, Curvilinear

EU-I-2 (Invited) 11:15~11:45

Development Of High-Brightness Xe LPP Source And Its Application

*이동근 (ESOL)

LPP EUV sources using Xe jets as targets havernthe advantage of producing less debris and having a relatively simple system.rnHowever, they have a drawback: they cannot create spatially localized plasmarndue to the effect of gas spreading in a vacuum. On the other hand, LPP sourcesrnusing solidified Xe targets can reduce the size of the plasma to the scale of-rnthe laser focus point, increasing brightness and efficiency in converting tornEUV light. But this also increases the cost of building and operating thernentire EUV source system because it requires an additional cryogenic system. Inrnthis development, we have created a localized high-density Xe target using anrnadvanced shocked nozzle instead of the traditional gas jet nozzle. By focusingrna laser on this target, we have developed a high-brightness EUV source. Wernintroduce this technology and present examples of its application in a spectrarnphotometry system. An actinic system that utilizes such a high-brightness andrnclean EUV source is expected to have high industrial applicability due to itsrnlow equipment cost and reduced maintenance expenses.

| Keywords : EUV Source, Xe LPP, EUV metrology

EU-I-3 (Invited) 11:45~12:15

Next-generation science and technology in EUV source

*김동언 (포스텍)

In the 21st century, quest has beenrngrowing about the study of how quantum systems evolve, and eventually, how torn-induce such quantum systems to behave as desired. In this sense, we arernentering a new scientific and technological paradigm, "Control Age."rnFor example, scientists would like to move electrons around during chemicalrnreaction processes that are far from equilibrium in a well-defined nanoscopic systems. The new era of science and technology calls for new tools to control electron behaviorrnin matters at the utmost time scale (femtosecond to attosecond) as well as to fabricate well-defined sub-nmrnscale nanoscopic systems. rnrn rnrnThe past two decades have witnessed thernremarkable advance in the new metrology for ultrafast electron dynamics, whichrnallows one to control material processes at electron level as recognized byrn2023 Nobel Prize in Physics, as well as for EUV lithography for well-defined nanoscopic systems. rnrn rnrnIn this talk, I share the excitement, reviewingrnrecent progress in the generation of ultrafast pulses (single cycle pulse, attosecondrnpulse, zeptosecond pulses) for real timernmeasurement and manipulation of electron dynamics in nanoscopic systems, as well as the advanced laser developmentrnfor more compact and efficient next-generation EUV sources.

| Keywords :
laser technology, attosecond science, technology, high-power solid state laser, next generation EUV source, blue x

EU-II
EUV Lithography II

13:30-15:00 KST, August 12(MON), 401/402

EU-II-1 (Invited) 13:30~14:00

High-NA EUV lithography and its challenge on depth of focus

*김황범 (SK hynix)

EUV scanner는 DRAM 산업계에 성공적으로 안착하였다. ArF-immersion scanner에서는 불가능했던 작은 pitch의 pattern에 대해서도 EUV scanner는 고유의 높은 해상력으로 single patterning을 가능케 했다. 이를 통해 multi patterning에서 야기되는 공정의 복잡성을 단순화시킬 수 있었다. 하지만 향후 tech node가 계속해서 감소함에 따라 EUV scanner로도 single patterning이 불가능해지고 더 높은 해상력을 가지는 High-NA EUV scanner를 필요로 하게 된다. High-NA EUV scanner에서는 NA가 0.33에서 0.55로 증가되며 기존에는 집광하지 못했던 고각의 회절광들을 집광하여 해상력이 높아진다. NA의 증가는 EUV beam의 반사율 감소를 야기하고 이를 완화하기 위하여 anamorphic 반사 광학계가 도입된다. Anamorphic 반사 광학계는 y 방향의 shot size를 반으로 감소시키며, AA 노광의 경우 사용 가능한 scribelane의 공간이 감소하고 AB 노광의 경우 in-die stitching 기술이 필요하게 된다.High-NA EUV scanner의 고각 회절광 집광 능력은 해상력을 높일 수 있으나 pattern의 DOF를 감소시킨다. Scanner의 focus control 능력과 장비 수차, wafer warpage 등은 focus의 불확실성을 불러 일으키며, 제품을 양산할 때는 충분한 focus margin이 필수적이다. Focus drilling은 DOF를 보다 증가시킬 수 있는 방법 중 하나이다. Scanning 속도에 맞추어 wafer stage를 상하로 움직일 경우 pattern의 focus에 의도적인 분포를 만들 수 있다. 이를 통해 defocus 영역에서 best focus에서의 높은 해상력을 빌려올 수 있으며, 결과적으로 DOF를 증가시킬 수 있다. 이에 high-NA scanner에서의 focus drilling을 통한 DOF 개선 가능성을 simulation을 통해 탐구한다.

| Keywords: High-NA, EUV, depth of focus, DOF, focus drilling

EU-II-2 (Invited) 14:00~14:30

Challenges of EUV Blankmask Technology in High NA EUV Lithography

*승병훈 (S&S TECH)

The advancement of semiconductor technologyrncontinues to drive the reduction in device sizes, necessitating the use of EUVLrn(Extreme Ultraviolet Lithography) technology for mass production of integratedrncircuits. With the ongoing transition from 0.33NA (Numerical Aperture) torn0.55NA lithography, it is imperative to develop EUV blankmasks suitable for thernHigh NA era. This development faces several technical challenges, includingrnsecuring the Depth of Focus (DoF) margin through the development of appropriaternmulti-layer, capping layer materials and structures, enhancing mask resolutionrnby creating new hardmasks for Optical Proximity Correction (OPC) assist bars,rnand improving mask registration via absorber stress control technologies. Thisrnstudy explores the development of EUV blankmasks for High NA EUVL, focusing onrnovercoming the aforementioned technical challenges.

| Keywords: High NA, EUV, Blankmask, Lithography

EU-I-3 (Invited) 14:30~15:00

EUV 포토마스크용 LTEM 소재

*김형준 (한국세라믹기술원, KICET)

In the 21st century, quest has beenrngrowing about the study of how quantum systems evolve, and eventually, how torn-induce such quantum systems to behave as desired. In this sense, we arernentering a new scientific and technological paradigm, “Control Age.”rnFor example, scientists would like to move electrons around during chemicalrnreaction processes that are far from equilibrium in a well-defined nanoscopic systems. The new era of science and technology calls for new tools to control electron behaviorrnin matters at the utmost time scale (femtosecond to attosecond) as well as to fabricate well-defined sub-nmrnscale nanoscopic systems. rnrn rnrnThe past two decades have witnessed thernremarkable advance in the new metrology for ultrafast electron dynamics, whichrnallows one to control material processes at electron level as recognized byrn2023 Nobel Prize in Physics, as well as for EUV lithography for well-defined nanoscopic systems. rnrn rnrnIn this talk, I share the excitement, reviewingrnrecent progress in the generation of ultrafast pulses (single cycle pulse, attosec-ondrnpulse, zeptosecond pulses) for real timernmeasurement and manipulation of electron dynamics in nanoscopic systems, as well as the advanced laser developmentrnfor more compact and efficient next-generation EUV sources.

MI-I
Advanced Metrology and Inspection I

10:45~12:15 KST, August 12(MON), 405/406

MI-I-1 (Invited) 10:45~11:15

Advanced Metrology Journey for Future Device Challenges

*한상현 (NOVA)

In recent years, the demand for AI-based systems in the semiconductor industry has surged, necessitating high-performance devices.

However, the scaling of semiconductor chips has reached its limits, increasing the demand for DTCO and STCO as paradigms to overcome these challenges. Approaches to enhancing device performance fall into two categories: innovating device architecture with 3D structures and enhancing system performance by integrating chiplets with advanced packaging. This paper will address the metrology technologies that meet the new challenges posed by these strategic directions in the semiconductor industry.

MI-I-2 (Invited) 11:15~11:45

Simulation-based MI and Digital Twin Technology for Semicoductor

*정재훈 (삼성전자)

As the physical structure of semiconductors continues to be scaled down to the nanometer level, it becomes increasingly difficult to accurately measure small changes in nano-sized elements. This has led to the widespread use of machine learning solutions in complex processes to achieve accurate and efficient measurement. However, machine learning models typically require hundreds of destructive inspection data sets, such as transmission electron microscope (TEM) images, which are not readily available. To address this issue, we have developed ViST-MI (Virtual Si Technology - Metrology and Inspection) solutions that use physics-based simulation results as data augmentation for spectrum and images. This approach allows for more accurate and efficient measurement of nano-sized elements, even with limited destructive inspection data sets. In this talk, we will present the ViST-MI technology and its applications that have been successfully applied in semiconductor metrology and inspection. We will also introduce a case study where silicon digital twin technology, built using ViST-MI, was used in semiconductor manufacturing.

MI-I-3 (Invited) 11:45~12:15

Exploring Generalization Capability of Deep Learning-Based Approaches for Holographic Image Reconstruction: Opportunities in Semiconductor Metrology & Inspection

*장무석 (KAIST)

On-axis holographic imaging is an imaging modality that poses an ill-posed problem of reconstructing complex-valued object functions from objects' diffraction intensity maps. Traditionally, this inverse problem has been solved based on iterative algorithms such as Gerchberg-Saxton (GS) algorithm and multi-height phase retrieval algorithm. Here, we will introduce some deep learning-based approaches to solve inverse problems in lensless imaging. This talk will focus on ways to incorporate physical forward models to solve inverse problems under perturbative configurations. It will further explore ways to extend the generalization capability of deep learning-based image reconstruction, including shape generalization, and discuss some opportunities of utilizing such generalization capability in semiconductor metrology & inspection.

MI-II
Advanced Metrology and Inspection II

13:30-15:00 KST, August 12(MON), 405/406

MI-II-1 (Invited) 13:30~14:00

Broadband Plasma Inspection Technology and Semiconductor High-Volume Manufacturing

*Sean Park (KLA)

BBP, broadband plasma, patterned wafer inspectors have pushed the boundaries of optical inspection to discover critical defects during chip manufacturing. Despite numerous challenges due to the physical limitations as the design rules continue to scale down, BBP wafer inspection products provide the most sensitive detection capability in the wafer level to manage the technical risk to manufacturing, and become an indispensable part of successful yield management. In this talk, we'll cover the evolution of BBP technologies, challenges of the patterned wafer inspection, how BBP inspection products push the boundaries of optical defect detection with sensors, optics, and advanced algorithms.

MI-II-2 (Invited) 14:00~14:30

Multiscale Thermal Metrology Bridging Nanoscale to Device Scale for Semiconductor Inspection

*장혜진 (서울대)

In the rapidly evolving field of semiconductor lithography, metrology and inspection now require an extended range of length scales along with a variety of properties to be examined. This talk introduces the fundamental principles of nanoscale thermal metrology and its application to multiscale metrology for semiconductor inspection. At the nanoscale, time-domain thermoreflectance based on an ultrafast pulsed laser system is employed to investigate thermal transport properties of thin material layers and interfaces within nanosecond timescales. The acquired thermal data serves as a foundation for understanding thermal behavior at larger scales and can further be correlated with physical, mechanical, and chemical properties. For example, the interfacial thermal conductance can inform the degree of adhesion of the buried interfaces. Transitioning to the micron scale, thermoreflectance microscopy enables visualization of temperature distributions over hundreds of micrometers at micron time scales. Finally, infrared thermography is utilized for millimeter-scale investigations. The multiscale approach, bridging nanoscale to millimeter scale, offers a powerful tool for semiconductor metrology, enhancing performance and ensuring the reliability of cutting-edge semiconductor devices.

MI-II-3 (Invited) 14:30~15:00

3D Tomography for semiconductor device manufacturing: the art of transforming an academic curiosity into an advanced metrology and inspection technique.

*Eugen Foca (Zeiss)

One of the main trends in the modern semiconductor architectures is 3D integration.

These new aspects of design span from very high aspect ratio structures in NAND devices over stacking of complex device elements in DRAM and logic to intricate material interfaces in advanced packaging.

One of the key questions associated with this change is what type of metrology and inspection techniques are required to support the future 3D scaling roadmaps? In our talk we bring in focus the 3D tomography performed with dual beam systems. During the past years, albeit being destructive, it effectively pushes its way from lab environment into near or in-line metrology and inspection in the fabs. We argue that this is the only technique which enables high resolution true 3D data extraction from advanced logic, NAND, and DRAM devices. We analyze the challenges associated with performing precise 3D metrology and inspection. Various case studies performed on NAND, DRAM and logic devices help positioning this approach onto the map of the current advanced process control technologies.

ET-I-1 (Invited) 13:30~14:00

Hard mask pattern processing for high aspect ratio contact etch

*이재원 (SK hynix)

High aspect ratio contact etching is a critical process in semiconductor manufacturing, aiming to create deep, narrow trenches or vias with high precision and aspect ratios. This study explores the application of hard mask pattern processing in achieving superior control and fidelity during high aspect ratio contact etching. In this research, we developed a novel hard mask patterning approach that enhances etch selectivity, minimizes etch bias, and ensures uniformity across the wafer. Detailed analysis of various hard mask compositions, including silicon-based and metal-based masks, was conducted to identify their etch resistance and compatibility with different etch chemistries. The implementation of multi-layer hard mask structures demonstrated significant improvements in maintaining critical dimensions (CD) and aspect ratios. A critical consideration in hard mask etching is the potential for defects induced by high voltage. These defects can significantly impact the integrity and performance of the etched features. Therefore, our study strongly emphasizes optimizing etch parameters to mitigate the risk of high voltage-induced defects. The findings suggest that hard mask pattern processing is a viable solution for achieving high aspect ratio contacts with enhanced accuracy and reduced defectivity, provided that careful attention is given to high voltage effects and complete mask opening. This work paves the way for the next generation of semiconductor devices, where precise patterning at the nanoscale is paramount. Future research directions include the exploration of novel hard mask materials and further refinement of etch processes to accommodate the evolving demands of semiconductor fabrication.

ET-I-2 (Invited) 14:00~14:30

A realistic 3D topography simulation platform for addressing emerging issues

*임연호 (전북대)

We have developed a realistic 3D feature profile simulation coupled with bulk plasma simulation to provide insight into the next-generation plasma process. For the effective development of a plasma chemistry database, we have characterized an inductively coupled plasma equipment using plasma diagnostic tools, including a cut-off probe, a Langmuir probe, and a quadrupole mass spectrometer. The reliability of the plasma bulk and surface reaction database for the simulation tools has been verified by plasma experimental data. Furthermore, we have developed a universal surface reaction model with a self-consistent numerical algorithm. Our surface reaction model is validated by comparing experimental data for the plasma of various FC gas species. We integrated this model into a 3D process simulator to investigate the veiled phenomena in the next-generation plasma oxide process. We demonstrate the integrated 3D feature profile simulations to understand specific abnormal behaviors during the plasma etching process such as bowing, necking, and profile distortions in the next-generation plasma oxide etching process. The concept of effective sticking coefficient, used in conjunction with our universal surface reaction model, is introduced to predict the realistic distribution of polymer radicals inside the nanoscale feature profile. Finally, we discuss the emerging issues of next-generation plasma oxide process using our realistic plasma process simulation.

Keywords :Plasma Process Simulation, Feature Profile Simulation, Plasma Etching

ET-I-3 (Invited) 14:30~15:00

Novel plasma sources for atomic scale etching

*정진욱 (한양대)

Ultra Low Electron Temperature (ULET) Plasma Sources for atomic scale etching

반도체 공정은 나노 규모에서 원자 수준으로 발전해오고 있습니다. 원자 수준의 공정을 위해서는 UV 방사선 손상, 이온 유도 손상, 전하 축적 손상 등을 최소화하기 위해 새로운 플라즈마 소스가 필요합니다. 이번 발표에서는 손상 없는 플라즈마 공정을 가능하게 하는 새로운 플라즈마 소스인 초저온 전자 온도(ULET) 플라즈마(Te < 0.5 eV)를 소개합니다. 또한 ULET 플라즈마를 생성하는 방법에 대해서도 설명할 것입니다. ULET 플라즈마에서는 높은 종횡비를 가진 패턴에서도 전하 축적이 거의 제거되고, 그래핀은 손상 없이 유지되는 반면, 기존의 플라즈마 공정에서는 심각한 손상이 발생합니다. ULET 플라즈마는 원자 수준의 플라즈마 공정 응용에 큰 가능성이 있습니다.

PM-I-1 (Invited) 13:30~14:00

Leveraging the strenghths of cyclic siloxane molecules and overcoming its weakness through the invention of a novel cyclic stannoxane molecule for EUV inorganic resist

*정현담 (전남대)

Hyeok Yun , Jiyoung Bang, Minyeob Kim(Department of Chemistry, Chonnam National University), Hyung-Bae Moon(4Chem Laboratory) Siwoo Noh(Pohang Accelerator Laboratory, POSTECH), Hee-Seon Lee, Kyuyoung Heo(Korea Research Institute of Chemical Technology), Ki-Jeong Kim(Pohang Accelerator Laboratory, POSTECH) Cheol-Min Kim(4Chem Laboratory)

EUV inorganic resists with unique molecular structures are essential to overcome the pattern collapse and meet the sensitivity, LER, and resolution requirements for advanced node semiconductors. To validate the concept of a condensable inorganic solid for generating chemical contrast within a dense inorganic network, the tetrahydroxy-tetramethyl-cyclotetrasiloxane (tetraol) molecule of octagonal structure was initially tested as an EUV resist material. While the condensation reaction between Si-OH groups, driven by electron-induced chemistry, enables the generation of chemical contrast and negative-tone patterns upon EUV irradiation, the lack of elements with high EUV photoionization cross-section in the molecule limits its EUV pattern performance and process margin. To leverage the strengths of the cyclotetrasiloxane resist and overcome its weaknesses, we have designed and synthesized a novel cyclic stannoxane molecule of octagonal structure through a reflux-based solution reaction, allowing for scalable production and molecular customization. Its molecular EUV photoionization cross-section is estimated to be five times larger than that of the cyclotetrasiloxane. We have confirmed the potential for fine line and space patterns to be realized in electron beam and EUV lithography with further optimization in the future. The octagonal cyclic stannoxane molecule we are proposing requires further analysis to more accurately determine its structure. However, if the structure is confirmed, it will be the first invention of its kind in the world. Given its expected outstanding mechanical properties, it is anticipated to be highly useful in various applications within the field of applied materials chemistry. Even when narrowing the focus to the field of EUV inorganic resist, recent experimental results suggest that if the purification process for synthesizing this material is developed, an appropriate underlayer for this material is created, and scientific understanding and optimization of the physical and chemical interactions at the resist-underlayer interface are achieved, it is expected that this material can actually be used in advanced node semiconductors.

PM-I-2 (Invited) 14:00~14:30

W-curve method to define photoresist resolution in EUV lithography

*서용범 (삼성전자)

As the semiconductor chip size continues to decrease, extreme ultra violet lithography (EUVL) is becoming an essential technology to achieve the high resolution patterning required for sub-7 nm node technologies. The patterning resolution of EUVL is highly dependent on the performance of EUV photoresists (PR) which can lead to variations in the patterning process and affects the overall quality of the semiconductor. Although there are several traditional methods to determine a patterning performance of PR, it becomes more challenging as scale tighten. To this end, we develop a new analysis method, named 'W-curve', defining EUV PR resolution using ADI SEM images, that visualizes bridge and -break defect cliffs and local CD uniformity at the same time. Using this method, different PR's performance at 36 nm-pitch line/space pattern was clearly distinguished. Also, the obtained result was well correlated with time-series trend data and electrical test data. Therefore, we believe that W-curve method could provide a new insight for understanding EUV PR resolution and help to design a new PR for higher patterning performance in a facile and versatile manner.

| Keywords: EUVrnlithography, photoresist, defect, stochastics

PM-I-3 14:30~14:45

Radical-driven Sensitivity Improvement of Tin-oxo Clusters for High NA extreme UV Lithography

*구예진 (인하대)

With advancements in extreme UVrnlithography (EUVL) with high numerical aperture (NA) optics, photoresist (PR)rntech-nology requires thinner films due to the limited depth of focus. Sincernthese thin films absorb fewer photons, the resist molecular structure should berndesigned to compensate for this, along with providing plasma etch resistance. Asrnwell as increasing the number of secondary electrons (SEs), it's crucial tornquickly reach the point where patterns form by promoting solubilityrnchanges in exposed regions, even with a limited number of photons and SEs. rnrnTo address this, an approach aimed atrnexpediting the solubility change in tin-oxo cluster (TOC) resist was proposedrnby promoting radical-based chemical reactions. This concept was experimentallyrnvalidated through the introduction of vinyl functional groups, which havern-excellent reactivity in radical-attacking reactions, into the underlayers and TOC structures. Our findings indicaternthat the introduction of unsaturated groups capable of forming bridging bondsrnwith radicals leads to a faster solubility change at a lower exposure dose,rnthus enhancing sensitivity. These results suggest a promising direction forrndeveloping resists tailored for high NA EUV lithography utilizing radical-basedrnchemical reactions

| Keywords:
EUV lithography, High NA lithography, Sensitivity, EUV resist, Underlayer, Tin-oxo cluster, Radical-based chemical reaction

PM-I-4 14:45~15:00

Advancing High-Resolution VIA Pattern through DSA and EUVL Integration

*윤세현 (전남대)

Vertical Interconnected Access (VIA) refers to contact hole patterns that are crucial in semiconductor systems by facilitating signal transmission across different circuit layers. As circuit scale continues to shrink, maintaining precise control over the accuracy of VIA pattern size and their placement becomes increasingly critical. One of the emerging lithography methods for sub-10nm pattern, the Extreme Ultraviolet Lithography (EUVL) method, still bounded by formation of defects in the pattern formation. Therefore, our study proposes an approach to improve VIA pattern quality by utilizing Directed Self-Assembly (DSA) of block copolymers, exploring different polymer architectures, on patterns generated by EUVL. By leveraging the inherent ability of DSA to form nanoscale periodic and orderly structures, our methodology aims to overcomes the limitations of EUVL. Through Monte Carlo simulations of Theoretical Information Coarse-Grained (TICG) model, our results demonstrate the effectiveness of DSA in rectifying EUV patterns with defects. The patterns are evaluated by roughness, number of missing holes, placement error, and size variations.

| Keywords:
Vertical Interconnected Access (VIA), contact hole, Extreme Ultraviolet Lithography (EUVL), Directed Self-Assembly (DSA), Simulation, Monte Carlo

PM-II-1 (Invited) 15:20~15:50

Multinuclear Tin-based Macrocyclic Organometallic Resist for EUV Photolithography

* 윤효재 (고려대)

We present a novel photoresist designed for extreme UV (EUV) photolithography, featuring a multinuclear tin-based macrocyclic complex. This photoresist comprises a trinuclear macrocyclic structure with three salicylhydroxamic acid ligands and six Sn-CH3 bonds, as confirmed through multinuclear nuclear magnetic resonance (NMR), FT-IR spectroscopies, and single-crystal X-ray diffraction studies. Demonstrating excellent stability against humidity, air, and thermal conditions, the resist also exhibits robust photochemical reactivity. Photochemical cross-linking was validated using X-ray photoelectron and solid-state NMR spectroscopic analyses. In EUV photolithography tests, a 44 nm-thick film on a silicon wafer achieved a line-edge roughness (LER) of 1.1 nm in a 20 nm half-pitch pattern. The Z-factor, which evaluates photoresist performance by balancing resolution, LER, and sensitivity (RLS), was calculated to be 1.28 × 10-8 mJ·nm3.

| Keywords : photoresist, organometallic, macrocycle, tin complex, EUV

PM-II-2 (Invited) 15:50~16:20

Sensitivity Enhancement of EUV Lithographic Patterning Using Tin-Containing Underlayer Materials

*이진균 (인하대)

13.5 nm 단파장 광원에 기반한 극자외선 리소그래피 (EUVL)는 화학증폭형 포토레지스트를 패터닝 소재로 이용하면서 본격적으로 양산공정에 적용되고 있다. 이러한 상황은 EUVL의 해상도(R)-패턴 거칠기(L)-감도(S) 간 상충 딜레마 완화에 유리한 새로운 레지스트 반응 메커니즘을 제안하는 데에 강력한 동기를 부여한다. 본인을 포함한 "인하대-포항가속기연구소-서울시립대-전남대" 공동 연구진은 탄소 (C)-불소 (F) 간 화학 결합의 이온화 방사선 조사 하에서의 분해 그리고 생성된 라디칼 간 결합 반응에 기초한 "불소화 EUV 레지스트" 개념을 제시한 후 연구를 진행해 왔다. 최근에는 주석산화물 나노 클러스터 코어에 불소화알킬 작용기를 결합시켜 새로운 레지스트 후보물질을 획득하게 되었다. 다단계 합성과정 및 음이온 치환과정을 통해 제조된 불소화알킬 주석산화물 나노 클러스터는 불소계 용제에 용해되어 균일한 박막으로 성형될 수 있었다. EUV에 노출된 나노 클러스터 박막은 불소화 작용기 간 결합 반응에 의해 용해도를 잃으면서 네거티브형 레지스트 패턴으로 변환되었다. EUVL 조건에서 대략 90 mJ/cm2 의 에너지 조사로 10 nm 이하 패턴 형성도 가능하다는 점을 확인하였다. 또한 불소계 재료 고유의 화학적 직교성 (Orthogonality)을 활용하여 다양한 소재의 언더레이어 위에서 적층 박막 형성이 가능하였고, 이를 통해 상당한 수준의 감도 향상을 관찰하였다. 본 발표에서는 불소화알킬 주석산화물 레지스트의 합성 및 특성 분석, EUV 조사 하 패터닝 특성 평가에 더해, 불소화 레지스트 소재와 비불소화 주석 화합물 언더레이어 (underlayer) 간 적층 박막 형성을 통해 EUVL의 감도 특성이 향상될 수 있다는 점을 계산화학과 실제 실험 결과를 비교하면서 보고하고자 한다

| Keywords : extreme UV, photoresis, underlayer

PM-II-3 16:20~16:50

Simulation Approaches for Exploring Process Conditions and Materials in EUV Lithography

*김현석 (전남대)

Despite recent significant advancements in extreme ultraviolet lithography (EUVL), achieving sub-10 nm patterning with reduced line edge roughness (LER) and improved sensitivity remains challenging, requiring extensive development of process conditions and resist materials. Our research is dedicated to optimizing these aspects to enhance EUVL performance, employing a patterning simulator for Chemically Amplified Resist (CAR) based on a coarse-grained model. We systematically explored the effects of various process conditions, including exposure dose and pattern size, across different pattern shapes such as line/space, contact holes, and tip-to-tip structures. Our model provides explicit simulations of molecular motions within the resist during the patterning process under varying conditions, correlating these dynamics to the final pattern quality. Furthermore, we examined changes in the chemical composition of polymer resists and the impact of molecular weight heterogeneity on the development process and LER. We also assessed the potential of inorganic resists and examined the role of underlayers in EUVL process.

| Keywords : EUV lithography, simulation, process condition, resist material

LO-I-1 (Invited) 13:30~14:00

Rigorous 3D Probabilistic Computational Lithography and Chip Level Inspection for EUV Stochastic Failure Detection

*김은주 (삼성전자)

Natural physical phenomena occurring at length scales of a few nm produces variation in many aspects of the EUV photoresist relief image: edge roughness, width roughness, feature-to-feature variability, etc. But the most damaging of these variations are stochastic or probabilistic printing failures. Stochastic or probabilistic failures are highly random with respect to count and location and occur on wafers at spectra of unknown frequencies. Examples of these are space bridging, line breaking, missing and merging holes. Each has potential to damage or destroy the device, reducing yield. Comprehensive detection is difficult: determination of frequencies can require massive metrology and is in many cases impractical. The problem presents formidable challenges yet valuable rewards to success. The underlying causes are complex. We believe the phenomena originates during exposure where quantized light and matter interact. EUV lithography is especially problematic since the uncertainty of energy absorbed by a volume of resist is much greater at 13.5 nm vs. 248 nm and 193 nm. The statistical fluctuation of quantized chemical components in the photoresist also contribute to defectivity. Complicated reactions during exposure, reaction-diffusion or condensation-diffusion and development may all affect the statistics of defectivity. In this paper, we use highly accelerated rigorous 3D probabilistic computational lithography and inspection to scan an entire N2 layout, predicting the location, type and probability of all stochastic printing failures with frequency of occurrence from 1E-9 to 1. The defect counting statistics for the layout are recovered and analyzed. Defects are classified by type and ranked by severity according to their probability of occurrence or by their contribution to counting statistics. We investigate how multiple optimized OPC solutions to an identical printing target differ in their predicted wafer defectivity. We investigate how perturbations to the lithography process and resist physical properties affect macroscopic defectivity. We show extensive data measuring agreement between simulated probabilities and experimental defect frequencies in N5 and N2 EUV processes.

| Keywords : EUV, computational lithography, computational inspection, stochastic defects, stochastic modeling, probabilistic modeling, stochastic failures, process optimization, OPC

LO-I-2 (Invited) 14:00~14:30

Expansion of Machine Learning Solution in OPC

* 김성호 (SK hynix)

Machine Learning is a subset of Artificial Intelligence (AI) that allows computers to learn data and improve through experience through various data instead of computer programming to solve problems. Machine Learning can set up various machine learning models depending on the type of data and desired results. Machine learning technology in the OPC (Optical Proximity Correction) field has initially been conservative in terms of improving OPC Runtime and OPC Model Accuracy, but machine learning problems such as overfitting and lack of data coverage are gradually decreasing with technological advances. Based on the strength of being able to use it as a tool to obtain desired results based on data, Machine Learning is expanding in to various area in OPC such as 1) Etch modeling which must consider not only DI (Development Inspection) CD (Critical Dimension) but also FI (Final Inspection) CD, 2) Hotspot Detection based on various Machine Learning features such as Optical, Geometry, and Density features, 3) CD-SEM Contour Extraction using Ensemble model. Because of Tech node shrinkage, OPC technology is gradually changing, nowadays machine learning is becoming a necessity, not a means.

| Keywords : OPC, Machine Learning, Etch modeling, Hotspot detection, Contour extraction

LO-I-3 (Invited) 14:00~14:30

300mm size Wire grid polarizer(WGP) manufacturing method using 50nm line pattern stitching process technology in ArF immersion

*송정철 (National NanoFab)

ArF immersion scanners are already quite advanced in the semiconductor field. However, it has not been applied to the Nano Materials industry, which requires unique structures and sizes. We explain how to produce optical products using an ArF immersion scanner. The large area wire grid polarizers (LA-WGPs) with 50 nm half-pitch were fabricated using ArF immersion lithography overcoming the limit of the shot field size. To realize the 50 nm line and space patterns on a 300 mm wafer, a zero-distance stitching process that connects the shot fields is suggested. To compensate for mutual interference between the shot fields which is called the local flare effect (LFE), the shot field arrangement is changed with optical proximity correction (OPC). Using a master wafer produced by the suggested method, 300 mm large-area WGPs were fabricated by the nano-imprint process.

| Keywords : ArF immersion, Stitching, Wire Grid Polarizer, Depth of Focus, Resolution, Photolithography

LO-II-1 (Invited, Online) 15:20~15:50

Computational Lithography of Metal-Oxo-Resists

*Ulrich Welling (Synopsys)

The ongoing miniaturization trend in EUV lithography necessitates the continued refinement of patterning targets, prompting an escalating demand for photoresist innovations. Concurrently, it is crucial to reduce exposure doses in order to minimize production costs.While chemically amplified resists (CAR) continue to enhance pattern fidelity through incremental improvements, alternative approaches are being explored as a means to achieve better results.Metal-Oxo-photoresists (MOR), which offer distinct characteristics for the described purposes, warrant thorough investigation. The fundamental differences between MOR and CAR manifest at multiple levels, including optical proximity correction (OPC) and possibly even at the design technology cooptimization (DTCO) stage.

| Keywords : EUV Lithography, MOR(Metal-Oxo-photoresist)

AL-I-1 (Invited) 13:30~14:00

Fabrication of mechanochromic structural color film through melt-shear assembly of a core-shell nanoparticles

*심태섭 (아주대)

Non-close packed colloidal crystals have been utilized as stimuli-responsive sensors because they change their optical properties in response to external stimuli. To create these structures, conventional methods have been used to form crystals by controlling delicate interparticle repulsion. In this talk, I talk about how to fabricate non-close packed colloidal crystals in facile manner by using melt-shear assembly of core-shell nanoparticles where the particles consist of a hard core and a soft shell. By diversifying the mechanical and optical properties of core-shell nanoparticles, I have shown that single particles can be used to create optical films with bright structure colors and different mechanochromic properties. Futhermore, a highly-sensitive mechanochromic strain sensor by using composite structures made of heterogeneous colloidal photonic crystal films are demonstrated.

| Keywords : Melt-shear assembly, Core-shell nanoparticles, Colloidal photonic crystals, Mechanochromism

AL-I-2 (Invited) 14:00~14:30

Direct and Indirect Photolithography of Quantum Dots

*강문성 (서강대)

Electroluminescencernfrom solution processed light-emitting materials such as quantum dots (QDs) orrnorganic luminophores is a suitable photon source for futuristic displaysrnoffering hyper-realistic images with free-form factors. Accordingly, arnnondestructive and scalable process capable of rendering multicoloredrnlight-emitting materials patterns on a scale of several micrometers needs to bernestablished. In this talk, two different nondestructive photopatterning methodsrnfor light-emitting materials, especially in focus on QD, are introduced, bothrnof which exploit crosslinking reaction between the ligands of neighboring QDs.rnThe first method exploits photoacivated crosslinking reacions. Using thisrnmethod, QD films can be directly photocrosslinked through a photomask, and therncrosslinked QD patterns can be formed after development step. This method isrnrefered to as the direct photopatterning methods. The second method alsornexploits the crosslinking reactions, but this time, it is activated with heat.rnIn this method, photoresist sacrificial patterns are first formed, QD films arerndeposited and thermally crosslinked, and then photoresist layers are stippedrnoff to leave QD patterns behind. Because this method avoids direct exposure ofrnQDs to light, we refer this method to as the indirect photopatterning method.rnDifferent aspects of these two different photopatterning methods will berncompared.

| Keywords : Quantum Dot, Display, Direct Photolithography, Indirect Photolithography

AL-I-3 (Invited) 14:30~15:00

Shadow growth for plasmonics

*정현호 (GIST)

This talk will present that nanoscale physical shadow growth offers various three-dimensionally shaped plasmonic nano-structures to be fabricated from a large library of materials, whose shapes can be engineered from simple spheres to complex molecular structures (including artifical oligomers, enantiomers, and rotamers) so that they exhibit unique optical properties.

| Keywords : nanomaterials, shadow growth, glancing angle deposition, plasmonics

AL-II
Alternative Lithography-II

15:20-16:50 KST, August 13(TUE), 403

AL-II-1 (Invited) 15:20~15:50

III-V/Si light source integration from on-demand to three-dimensional dimensions.

*노유신 (건국대)

Despite the substantial progress being made in Si-based light modulationrnand detection and their large-scale, cost-effective, monolithic devicernintegration technology, the realization of small, efficient, and reliable on-chiprnintegrated light sources, for example, continuous-wave (CW) III-V semiconductorrnnanolasers and electrically driven micro-/nanoLEDs on Si at room temperaturern(RT) has remained a challenge due to the lack of appropriate integrationrnschemes. Here, we introduce a simple, easy and damage-free micro-transfer-basedrnmanipulations that enables the realizations of on-demand Si-integrable RT CW nanolasers,rnelectrically driven on-chip transferrable micro-/nanoLEDs and verticallyrnheterogeneous integrable three-dimensional (3D) III-V/Si micro-resonators/lightrnsources. A smartly designed InGaAsP gain structure in conjunction with anrnindividually addressable and highly precise on-demand gain-printing techniquernaddresses several key technological issues, demonstrating the RT CW operationrnwith a low-thresholds of ~50 μW, the all-graphene-contact-assistedrnelectroluminescence, and the spontaneous emission and its enhancement in 3D wood-pile-type PhCrnnanocavities. A simplerndemonstration of the on-demand gain-printing and the integrated Si-integrablernlight sources exhibit the potential of wide and ubiquitous adoption in Sirnphotonics and photonic integrated circuit (PIC) communities

| Keywords : Transfer-printing, III-V/Si integration, nanoscale light sources, photonic crystals, microdisks

AL-II-2 (Invited) 15:50~16:20

Co-integration of zero-static-power nanomachines with silicon photonics

*한상윤 (DGIST)

Silicon photonics is rapidly emerging as arntransformative technology with applications in real world. However, the currentrn-silicon photonic devices often require high power consumption and have not yetrnreached their fundamental limits in integration density. This is mainly due torntheir inefficient modulation mechanisms, which demand both high power and largern-footprints. In this presentation, I will discuss the latest advancements inrnintegrating electrostatic nanomachines with silicon photonics. This integrationrnleads to the development of silicon photonic circuits characterized by nearlyrnzero-static-power consumption, high integration density, and minimal footprint,rnachieving highly efficient tuning over shorter distances.

| Keywords : Silicon photonics, zero-static-power, nanomachine, co-integration

AL-II-3 (Invited) 16:20~16:50

Advanced Nanofabrications for Nanophotonics: 3D EBL, Single-digit Nanometer Scale EBL and scalable NIL

*김인기 (성균관대)

본 발표에서는 전자빔 리소그래피와 나노임프린팅 리소그래피를 활용한 메타물질 가공 기술들을 소개하고자 한다. 메타물질 및 메타표면을 활용한 광 제어 기술 및 이를 활용한 디바이스 응용 분야가 확장됨에 따라 리소그래피 기술에 대한 관심이 더욱 커지고 있다. 기존에 잘 알려진 전자빔 리소그래피 및 나노임프린트 기술 등을 활용 및 변영하여 기존에는 구현하기 어려웠던 새로운 형태의 나노포토닉스 디바이스를 구현한 결과들을 소개하고자 한다. 구체적으로, 1) 전자빔 리소그래피 오버레이 기술을 활용한 3차원 메타물질 및 온-칩 메타표면 제작 기술, 2) 연속 도미노 공정을 활용한 한 자릿수 나노미터 스케일의 플라즈모닉스 구조 제작 기술, 3) 나노입자 복합재와 연속 나노임프린팅 기술을 활용한 메타표면 대량 생산 기술 등의 기술을 소개하고자 한다.

| Keywords : 전자빔 리소그래피, 나노임프린트, 3차원 메타물질, 온-칩 메타표면, 플라즈모닉스

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Poster Presentation Session

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포스터 세션 (둘째날 오전 9시 - 10시 30분) 에는 질문에 답하실 수 있도록 자리를 지켜주시기 바랍니다.

PS1 - EUV Lithography

PS1-01

Underlayer dependent local wafer deformation during EUV exposure

*고희창 (Hanyang Univ)

리소그래피 공정에서 중요한 역할 중 하나는 포토레지스트에 최적의 선량을 전사하여 집적 회로의 패턴을 제작하는 것입니다. 패턴 형성에 필요한 선량은 불가피하게 국부적인 온도 상승을 유발하여 열 변형을 초래합니다. 이 과정에서 thermal actuator 를 사용하여 노광의 영향을 완화하려는 시도가 이루어졌습니다. 그러나 웨이퍼의 가열 문제는 사용된 하층막 구조와 재료에 따라 다이와 웨이퍼 전체에 걸쳐 열 변형이 다르게 발생한다는 점에서 기인합니다. 동일한 선량에서도 하층막 구성에 따라 발생하는 열 변형의 차이는 오버레이 예산을 크게 제한할 수 있습니다. EUV 스캐너 환경에서 다양한 하층 재료와 구조에 따라 열 변형을 유한 요소 분석 방법으로 시뮬레이션했습니다. 공개된 하층막 구조에 대한 시뮬레이션을 통해 하층막이 웨이퍼에 더 많이 증착될수록 열 변형이 점진적으로 증가하는 것을 확인하였습니다. 특히 메모리 공정에 사용되는 하층막 구조의 경우, 다이 내에서 최대 2 nm 이상의 변형이 발생하였습니다. 이는 하층막의 사용 조건에 따라 같은 공칭 조건에서도 열 변형의 차이가 1 nm 를 초과할 수 있음을 시사합니다.

| Keywords : EUV scanner, Wafer heating, Overlay, EPE

PS1-02

Improving Process Window and Resolution through Polarization in High NA EUV

채유진, 김민우, 유다경, 손승우, *오혜근 (Hanyang Univ)

The semiconductor industry is currently transitioning to advanced extreme-ultraviolet lithography (EUVL) to address the challenges facing the use of photolithography in microprocessor and memory chip integration. This shift has sparked a surge in novel inorganic EUV photoresist research. However, several technical issues, such as insufficient EUV sensitivity, poor understanding of the photochemistry, and poor stability, have emerged. Here, the EUV sensitivity and stability of state-of-the-art tin oxo clusters are enhanced by integration with the photoactive nitrate anion to give [(BuSn)12O14(OH)6](NO3)2 (TinNO3). The findings of the study reveal that nitrate anions in TinNO3 showing the photosensitivity as low as 32 mJ/cm^2 and maintaining stability irrespective of the post-exposure environment. Furthermore, TinNO3 possesses superior resistance to dry etching, enabling selective etching of Si and the amorphous carbon layer. Finally, through intensive optimization of the post-exposure bake parameters, photoresist-substrate adhesion, and development conditions, well-ordered CD 45 nm L/S patterns of TinNO3 thin-film were achieved using ArF lithography.

Keywords: 극자외선 노광공정, 입자 결함, 펠리클, 회절 패턴, 임계 치수, EUV 광 파장 검사, 이미징 성능 변화

PS1-03

Enhancement of photosensitivity and stability of Sn-12 EUV resist by integrating photo-active nitrate anion

강여경, *김명길 (SUNGKYUNKWAN Univ)

The semiconductor industry is currently transitioning to advanced extreme-ultraviolet lithography (EUVL) to address the challenges facing the use of photolithography in microprocessor and memory chip integration. This shift has sparked a surge in novel inorganic EUV photoresist research. However, several technical issues, such as insufficient EUV sensitivity, poor understanding of the photochemistry, and poor stability, have emerged. Here, the EUV sensitivity and stability of state-of-the-art tin oxo clusters are enhanced by integration with the photoactive nitrate anion to give [(BuSn)12O14(OH)6](NO3)2 (TinNO3). The findings of the study reveal that nitrate anions in TinNO3 showing the photosensitivity as low as 32 mJ/cm^2 and maintaining stability irrespective of the post-exposure environment. Furthermore, TinNO3 possesses superior resistance to dry etching, enabling selective etching of Si and the amorphous carbon layer. Finally, through intensive optimization of the post-exposure bake parameters, photoresist-substrate adhesion, and development conditions, well-ordered CD 45 nm L/S patterns of TinNO3 thin-film were achieved using ArF lithography.

| Keywords : Extreme-ultraviolet lithography (EUVL), EUV photoresists, Tin oxo clusters, Nitrate anions, Nano-patterning

PS1-04

Mask 3D effect의 완화를 위한 high-NA 용 EUV 마스크 흡수 소재 탐색 연구

이승호, 정동민, 김연수, *안진호 (Hanyang Univ)

EUV 노광공정(Extreme ultraviolet lithography)은 반도체 소자의 미세화를 구현하기 위한 필수 기술로 주목받고 있으며, 3 nm 노드 이하의 반도체를 구현하기 위해 high-NA 시스템이 도입되고 있다. 그러나, 기존의 TaBN 마스크를 high-NA 시스템에 적용할 경우, 두꺼운 두께로 인해 M3D effect(Mask 3D effect)가 극심해지고 이미징 성능이 제한되기 때문에 이를 대체할 EUV 마스크 흡수 소재의 개발이 필요하다. 이에 M3D effect의 완화를 통해 이미징 성능을 향상시킬 수 있는 광학상수 영역을 제안한다. PROLITH 2023a 광학 시뮬레이션을 평가에 활용하였으며, 5.355°의 입사각, central obscuration 및 anamorphic optics의 high-NA 시스템 환경을 적용하였다. 14 nm line and space의 수직 및 수평 패턴에 대해 30 nm에서 40 nm 사이의 두께로 평가를 진행하였으며, M3D effect의 주요 요소인 best focus shift 및 telecentricity error에 대해 평가하였다. Best focus shift의 경우, 수직 및 수평 패턴 모두 0.030이상 0.090이하의 소광계수(Extinction coefficient, k) 및 0.990이상 1.01 이하의 굴절계수(Refractive index, n)를 가지는 near n≈1.0 영역에서 10 nm 이하의 완화된 값을 가지는 것을 확인하였다. 또한, telecentricity error 평가 결과, 사입사의 영향이 없어 전체적으로 0의 값을 가지는 수직 패턴과 달리 수평 패턴은 0.080이하의 k 및 near n≈1.0 영역에서 0.75 mrad의 완화된 값을 가지는 것을 확인하였다. 결과적으로, near n≈1.0 영역에서 best focus shift 및 telecentricity error 모두 완화되는 것을 확인하였으며, 해당 영역의 소재를 활용할 경우 M3D effect를 완화할 수 있을 것으로 예상된다.

Keywords : EUV lithography, High-NA system, EUV mask, Imaging performance, Mask 3D effect, Best focus shift, Telecentricity error

PS1-05

EUV ptychography microscope를 이용한 주기성 마스크 패턴의 고신뢰성 actinic 검사를 위한 EUV ptychography imaging 연구

홍준호,이동기,문승찬 , *안진호 (Hanyang Univ)

극자외선 노광기술(Extreme ultraviolet lithography)은 3 nm node 이하 공정에 적용되기 위해 활발히 개발되고 있으며, 이에 고해상도의 패턴 마스크 검사 기술 개발 역시 수반되어야 한다. EUV 계측 분야에서는 광 특성으로 인한 고효율의 이미징 광학계를 구성하는데 어려움이 있어 coherent diffractive imaging (CDI) 방법을 이용한 actinic 패턴 마스크 검사 연구가 활발히 이루어지고 있다. 그러나 이 역시 매우 반복적인 주기성 패턴에 대해서는 이미징에 어려움을 겪고 있다.본 연구에서는 고차조화파 방식으로 생성한 coherent EUV 광, 6° 사입사 조명 광학계를 탑재한, CDI 기반의 actinic 패턴 마스크 검사 장비인 EUV ptychography 현미경을 사용하였으며, multi-shot CDI의 한 종류인 ptychography 방식으로 주기성 패턴에 대한 이미지 복원 성능 개선 연구를 진행하였다. 이는 위상복원 알고리즘의 update function에 복원 정확도 및 속도 개선을 위한momentum항을 추가하고, object와 probe 사이의 crosstalk 에러를 최소화하기 위한 modulus enforced probe (MEP)을 결합함으로써 수행되었다. 개선된 알고리즘의 성능 확인을 위해, far-field 영역에서 획득한 200 nm half pitch dense line 회절 패턴에 대하여 amplitude map과 phase map을 재복원하고 이를 대조하였다.그 결과, 개선된 알고리즘의 iteration에 따른 Fourier error를 통해 복원 정확도는 약 26 %, 수렴 속도는 약 1.8배 이상 개선되었음을 확인하였다. 또한 EUV mask의 흡수체와 반사체 간의 측정된 위상 차이는 0.98 π로, 이론적 수치인 0.96 π 와 매우 근사하였다. 결론적으로, EUV ptychography 현미경의 주기성 패턴의 actinic 검사에 대한 실효성을 입증하였으며, 차세대 EUV 마스크의 성능 평가 장비로의 활용 가능성을 확인하였다.

Keywords : EUV lithography, Actinic pattern mask inspection, Coherent diffractive imaging, EUV ptychography

PS-1-6

Spectral analysis of short-wavelength emissions for characterizing Tin laser-produced EUV light sources

손장협, 조병익 (GIST)

Tin laser-produced plasmas (LPPs) are critical sources of extreme ultraviolet (EUV) light used in state-of-the-art EUV nanolithography. In pursuit of enhanced EUV light sources, Nd:YAG or thulium solid-state lasers have been considered as potential alternatives to CO2-gas lasers, currently employed to drive tin plasmas in EUV lithography machines. However, significant challenges arise in diagnosing and modeling short-wavelength LPPs due to spatiotemporal inhomogeneity and complex emission and absorption spectra from numerous transition lines. Here, we characterize EUV light sources using measured short-wavelength emissions (7-11 nm), where contributions from various charge states can be resolved, by fitting them with results from non-local thermodynamic equilibrium (NLTE) collisional-radiative calculations and radiation-hydrodynamic simulations. The agreement between the calculated and measured spectra allows for diagnosing the effective temperatures of plasmas and establishing their relationship with laser intensity, which helps estimate the optimal laser intensity.

Keywords : Laser-produced plasma (LPP), Extreme ultraviolet (EUV), short-wavelength emission, non-local thermodynamic equilibrium (NLTE), collisional-radiative calculation, radiation-hydrodynamic simulation

PS-1-7

수직 분자설계된 EUV 레지스트의 화학 기상 현상 기반 건식 현상 성능 평가

김지원, 석지후, 지현석, 이재혁, 윤광섭, 성명모, *안진호 (Hanyang Univ)

최근 반도체의 고집적도에 대응하기 위해 High-NA EUV 리소그래피 기술의 도입이 진행되고 있다. High-NA EUV 리소그래피가 적용됨에 따라 DOF(Depth Of Focus)는 작아지므로 초고해상도 패턴 형성을 위해 레지스트 소재 및 공정 연구가 필수적이다. 우리 연구팀은 유기-무기 분자층 다층막이 수직분자선 구조를 갖도록 설계한 새로운 개념의 EUV 레지스트 소재를 개발하여 낮은 선단거칠기, 높은 감도, 우수한 내 에칭성을 확보하는 결과를 발표한 바 있다. 현재 EUV 레지스트 분야에서는 RLS(Resolution, Line width roughness,rnSensitivity) trade-off를 개선하는 것뿐만 아니라 패턴 붕괴 결함을 극복하는 것이 과제로 남아 있다. 최근 패턴 붕괴를 방지할 수 있는 건식 현상 공정이 초고해상도 패터닝을 위한 핵심 기술로 떠오르고 있다.rnrn본 연구에서는 화학 기상 현상(Chemical Vapor Development, CVD) 공정을 수직 분자 설계된 유기-무기 하이브리드 다층막 EUV 레지스트에 적용하여 패터닝 성능을 확인하였다. Half pitch 25 nm, 50 nm, 100 nm, 500 nm Line andrnspace 전자빔을 통해 노광한 패턴이 현상 증기에 의해 현상되어 균일한 패턴을 형성한 결과를 확보하였다. 본 연구는 수직 분자 설계된 유기-무기 하이브리드 EUV 레지스트에 적합한 건식 현상 공정 기술을 제안하며, 향후 패턴 붕괴 없이 고해상도 레지스트 패턴을 구현할 수 있을 것으로 기대한다.

Keywords : Extreme ultraviolet lithography, EUV photoresist, MOR, Dry photoresist, Dry development process, Chemical vapor, Patterning performance

PS-1-8

Challenges of Mask Blank Technology in High NA EUV Lithography

박민규, 우미경, 윤종원, 양철규 (에스엔에스텍)

반도체 기술의 발전은 소자의 크기가 줄어드는 방향으로 지속되고 있으며, 이에rn따라 집적회로 양산에 필요한 EUVL(Extreme Ultraviolet Lithography) 기술이rn도입되어 사용되고 있다. 이에 더해, EUVL 기술은 현재의 0.33NA(Numerical Aperture)에서 0.55NArnLithography의 시대로 변화가 진행되고 있다. 따라서, EUV Lithography에서 중요한 재료 중 하나인, Blankmask는 High NA 시대에 맞는 개발이 요구되고 있다. High NA에rn적합한 EUV Blankmask 제조에는 여러 기술적 도전과제가 있다.rn기술적 도전과제로 DoF Margin 확보를 위한rnMultilayer/Capping layer의 물질 및 구조 개발, Mask Resolution 향상rn목적의 OPC Assist Bar 형성을 위한 New Hardmaskrn개발, 그리고 Mask Registration 향상을rn위한 Absorber stress 제어 기술의 개발이 있다. 따라서, 본 연구에서는 앞서 언급된 3가지 도전과제에 대해 High NA EUVL 적용을 위한 EUV Blankmask 개발 방향을rn연구하였다.

Keywords :EUV Lithography, High NA, 0.55NA, PSM, Simulation, Process, Mask blank

PS-1-9

EUV 펠리클 제작을 위한 Si 습식 식각 공정 시 발생하는 오염물의 제어 연구

김태환, 김하늘, 김정연, 강영우, 박영욱, *안진호 (Hanyang Univ)

EUV 펠리클은 노광 공정 도중에 발생하는 오염물로부터 mask를 보호하며 반도체 제조 공정의 수율을 높여 준다. EUV 펠리클을 제작할 때 Si를 용이하게 제거하기 위해 주로 습식 식각 공정이 적용되고 있다. 하지만 습식 식각 공정을 진행할 때 패턴의 하부가 식각되는 undercut 현상이 발생하고, 이러한 현상이 발생하는 edge 및 corner 부분의 상부막이 탈락하여 펠리클의 오염원으로 작용할 수 있다. 본 연구에서는 EUV 펠리클 제작 간에 일어나는 undercut 현상을 개선하기 위해 compensation 구조 증착을 진행하여 추가적인 geometry를 형성하였다. 실험 진행은 다음과 같다. 8-inch Si wafer 양면에 LPCVD SiNx를 증착 후 backside에 membrane 영역과 scribe line을 형성한 다음, membrane edge 및 corner 부분에 compensation 구조를 증착한다. Compensation 구조 조건은 corner의 경우 <100>-beam과 square type 구조를 선정하였고 edge의 경우 10~50 μm 너비의 line geometry를 각각 적용하여 세분화하였다. Compensation 구조 물질은 식각 용액인 KOH와의 선택비를 고려하여 PECVD SiO2를 증착하였다. 최종적으로 wet etching을 진행하여 undercut 개선 효과를 측정하였다. 식각 결과 평가는 optical microscopy 분석을 이용하여 진행하였다. 측정 결과 corner의 경우 square type 구조의 결과가 기존에 발생하던 1.6 mm길이의 undercut 현상을 완전히 개선하였고, edge의 경우 35 μm이상의 내부 compensation 구조 형성 시, 16 μm 길이로 형성되던 undercut이 발생하지 않도록 개선됨을 확인하였다. 결과를 통해 Si wet etching 공정에서 발생하는 undercut 현상을 제어하기 위한 최적 구조를 설계하였고 오염물 제어 효과를 확인하였다.

Keywords : EUV pellicle, Si wet etching, Fabrication process, Sacrificial layer, Undercut, Contamination, Compensation structure

PS-1-10

Variation of Photosensitivity in Antimony-Based Organometallic EUV Photoresists According to Ligand Position

이선진 (SUNGKYUNKWAN Univ)

As the microelectronics industry follows Moore's Law, advanced photoresists are increasingly demanded. This study presents an antimony-based organometallic negative-tone resist to tackle EUV lithography challenges. Optimized through strategic ligand position adjustments, this resist shows precise nanopatterning capability, suggesting its potential as a superior alternative in semiconductor manufacturing.

Keywords : EUV Lithography, photoresist, antimony-based organometallic, sensitivity, ligand position

PS-1-11

EUV Pellicle 의 상대적 수명 추정: 피로 해석을 통한 소스 전력 및 결함의 영향 비교

전지현, *오혜근 (Hanyang Univ)

극자외선(EUV) 리소그래피에서 펠리클은 반도체 제조의 수율 및 처리량을 최대화하는 데 중요한 역할을 한다. 그러나 얇은 구조로 인해 열, 압력 오염, 물리적 손상 등에 민감하다. 이로 인해 펠리클의 성능과 수명을 크게 좌우되며, 실제 스캐너 환경에서 펠리클의 수명을 정확히 예측하는 것은 어렵다. 기존 연구에 따르면 펠리클의 기대 수명은 10,000 웨이퍼 이상으로 알려져 있지만, 이를 기준으로 펠리클의 수명을 직접적으로 평가하기는 어렵다. 펠리클의 수명은 펠리클의 구조적 차이, 외부 요인의 다양성, 측정 방법의 차이, 재현성의 문제 등 여러 요인에 따라 달라지기 때문이다. 따라서 EUV 펠리클 수명을 예측하고 펠리클 교체 시기를 결정하는 것은 매우 어렵다. 펠리클의 대략적인 상대적 수명이라도 수명을 추정할 수 있다면 매우 유용할 것이다. 소스 전력 250 W 에서 보고된 펠리클의 수명은 pSi의 경우 1K 웨이퍼, MoSi2의 경우 10K 웨이퍼, CNT의 경우 100K 웨이퍼로, 본 연구에서는 이를 기준으로 수명을 추정하였다. 현재의 EUV 노광 조건에서 펠리클이 받는 열 응력을 시뮬레이션을 통해 계산하였고, 각각의 UTS로 정규화하여 나타내었다. 따라서 보고된 펠리클의 수명과 계산된 열 응력을 통해 다양한 펠리클 구조, 소스 전력 및 입자 결함에 대한 EUV 펠리클의 상대적인 수명을 대략적으로 추정하고자 하였다.

Keywords : EUV lithography, EUV Pellicle, Pellicle lifetime, Particle defect, Pellicle thermal stress, Source power, Residual stress

PS-1-12

Development of performance evaluation system for extreme ultraviolet (EUV) materials

김우람, 최은석, 제갈원, 강상우, *김정형 (KRISS)

In advanced semiconductor manufacturing industries, extreme ultraviolet (EUV) based lithography has become a key technology to transfer ultrafine patterns on logic and memory devices for high-performance computational chips. EUV materials must be developed for photoresists, pellicles, and mirrors to print accurate circuit patterns on wafers. An EUV performance evaluation system that can quantitatively evaluate the performance of optical sensitivity, transmittance, reflectance, and uniformity must be established. In this work, we demonstrate the EUV performance evaluation system for photoresists. It consists Z-pinch-based EUV light source, an optical system, and a testing bed. EUV light source is optimized to enhance optical power with a wavelength of 13.5 nm and the optical system is configured with two mirrors with an angle of incidence of 5 degrees. Testing beds can be designed to fix the two types of samples with absorption and transmission. An optical fluence at the testing bed is 30 mJ/cm2 and verified by printing line and space patterns on EUV photoresist. Therefore, the EUV performance evaluation system can be widely used to measure optical characteristics of EUV materials such as photoresist.

Keywords : EUV, inspection, photoresist

PS2-01

Depth Estimation Using Multi-modal Deep Learning from SEM Image and OCD Spectrum

황예은, 송민서 (SOGANG Univ), 마아미, 김규환, 장규백, 정재훈, 김대신 (SAMSUNG), *강석주 (SOGANG Univ)

반도체의 공정 과정에서 반도체의 구조를 정확히 파악하는 것은 매우 중요하다. 최근 인공지능 기술의 발전으로 scanning electron microscope (SEM) 영상을 활용한 반도체 깊이 추정 연구가 활발히 진행되고 있다. 그러나 단일 SEM 영상에는 절대 깊이 정보가 충분하지 않아 정확한 구조 계측이 어렵다. 본 연구에서는 이러한 한계를 극복하는 방안으로SEM 영상과 optical critical dimension (OCD) 계측 방법을 활용한 멀티모달 기반의 구조 예측 딥러닝 프레임워크를 제안한다. 제안하는 프레임워크는 SEM 영상과 OCD 스펙트럼 데이터에 적합한 인코더를 설계하여 멀티모달 기반의 깊이 추정 네트워크를 통해 반도체 구조를 예측한다. 실험 결과, 다중 데이터를 이용한 구조 예측 방법이 단일 데이터를 이용하는 방법에 비해 예측 값과 실제 값 사이의 오차를 59%가량 감소시켰음을 확인하였다.

| Keywords : scanning electron microscope (SEM), optical critical dimension (OCD), multi-modal deep learning, metrology

PS2-02

Polarization-sensitive Fourier Ptychography via Pupil Plane Multiplexing

채혜숙, 이경원, 윤한솔, 이경철, *이승아 (YONSEI Univ)

We present a novel polarization-sensitive Fourier Ptychographic Microscopy (FPM) method that leverages multiplexing techniques in the Fourier plane, eliminating the need for costly polarization cameras or mechanical polarizer rotations. By simply introducing semicircular 0° and 90° linear polarizers in the Fourier plane of a conventional FPM setup, we can effectively split a single pupil into two half-circle pupils, enabling the simultaneous multiplexing of two channels' signals within a single measurement. By imposing two pupil functions on FP phase retrieval, we reconstructed the amplitude and phase information of the two orthogonal polarization channels, ultimately obtaining the Jones matrix of the anisotropic specimen. To validate our proposed method, we demonstrate its application by accurately reconstructing the orientation of the slow axis and phase retardation of MSU crystals known as the birefringence object.

| Keywords : Fourier ptychography, multiplexing, polarization, birefringence, phase retrieval

PS2-03

Multiplexed Fourier ptychography with analytical pupil reconstruction for enhanced imaging

나현서, *장무석 (KAIST)

Fourier ptychography microscopy (FPM) is a computational imaging technique that achieves both wide field of view and high resolution. In contrast to the transmission mode, the reflective mode has gained prominence as a method for surface inspection in industrial applications. However, the practical application of this technique is challenging due to limitation in acquisition speed and accuracy. Previous studies used multiplexed illumination to overcome this limitation, but many iterations were required for correct field reconstruction. This study achieves complex field reconstruction with fewer iterations by combining the analytically obtained pupil in the reconstruction process. We sequentially acquire brightfield measurements to retrieve the complex aberrations of the imaging system, and then use these aberrations to iteratively reconstruct multiplexed darkfield measurements. Compared to the conventional multiplexed reconstruction, our strategy achieves robust complex field in fewer iterations and is less sensitive to the optimization parameters.

| Keywords : Fourier ptychography microscopy(FPM), Multiplexed illumination

PS2-04

High NA Catadioptric 대물렌즈의 광학 설계 및 성능 분석

조유빈, Joo Ji Yong, Park Ji Hyun, * Lee Jun Ho (Kongju Nationa Univ)

반도체 및 디스플레이 산업이 발전할수록 회로 선폭을 더욱 미세화되고 있으며 이에 따라 MI(Metrology & Inspection) 공정에서도 고분해능의 광학계가 요구되고 있다. 하지만 국내에서는 낮은 파장 대역에서 사용 가능한 High NA 대물렌즈의 개발 경험이 적어 전량 수입에 의존하고 있다. 국내 원천 기술 개발을 위해 DUV 파장(193nm)에서 사용 가능한 NA 0.9인 검사용 대물렌즈의 광학 설계와 성능 분석을 진행하였다.본 논문에서는 문헌 조사를 통한 NA 0.9 대물렌즈의 설계 타입 선정과 국내 렌즈 제작 기술을 고려한 최적 설계 진행, 온도 민감도 분석을 통한 실환경 운용 가능성, 설계된 렌즈의 예상 수율 및 할당 공차를 파악하기 위한 민감도 분석 진행 결과를 소개한다.

| Keywords : DUV, High NA, Objective Lens, Metrology & Inspection, Tolerance

PS2-05

Meta Shack-Hartmann wavefront sensor with enhanced spatial resolution and acceptance angle for incoherent phase imaging

송국호, *장무석 (KAIST)

Shack-Hartmann Wavefront Sensors (SHWFS) are composed of a grid of microlenses, each measuring the local wavefront gradient in its area based on focal spot displacement. Compared to interferometric phase measurements, its optical setup is extremely simple and stable, and it does not require coherent plane wave illumination. However, conventional SHWFS based on MEMS-fabricated microlenses has significant limitations in lenslet density and curvature, preventing it from achieving adequate phase imaging performance for metrology or biomedical imaging applications. To overcome these limitations, we have introduced a metasurface-based SHWFS technology aimed at implementing lenslet parameters that can surpass these constraints. Experimentally, we have implemented an SHWFS with a spatial resolution of 12.95μm and an acceptance angle of ±8°, representing 100× better spatial resolution and 10× larger operating angle compared to conventional SHWFS systems. We also have validated snapshot phase imaging for complex-shaped objects and successfully tracked the 3D position of incoherent sources. Our approach offers the opportunity to add phase sensing capabilities to existing optical equipment by simply replacing conventional intensity-only light sensors, without requiring significant changes to form factor or additional setup.

| Keywords : Metasurface, Shack-Hartmann Wavefront Sensor, Phase imaging, Wavefront sensing, Incoherent source, Metrology

PS2-06

Noise-robust kernel estimation based blind deblurring method for metrology and inspection

이찬석 (KAIST)

Scanning electron microscopes (SEM) provide sub-nanometer resolution images, playing a crucial role in metrology and inspection within the semiconductor fabrication process. However, incident electrons, which determine the shape of the SEM's point spread function (PSF), can be easily distorted and blur the image. Also, random fluctuations of the incident electrons cause Gaussian noise, significantly compromising image quality. Correcting such degradation requires manual adjustment of system parameters by experts. Also, several image quality assessment-based methods have been proposed to automate such correction process. However, these methods require iterative measurement that are time-consuming and energy-inefficient. Here, we propose a single-shot image correction method, i.e. blind deblurring, which is based on a noise-robust kernel estimation function and deep image prior (DIP). Specifically, the proposed kernel estimation function effectively estimates the PSF even for strongly noisy blurry image, given a clear image and constant noise suppression factor. To reconstruct a clear image, DIP, which has a strong prior in generating a natural image, is introduced. Additionally, the multiple kernel estimation scheme is designed to address a wide range of unknown noise levels. The proposed method shows outstanding deblurring performance and is expected to pave the way for new advancements in SEM image correction.

| Keywords : Scanning electron microscopy, Blind deblurring, Deep learning, Gaussian noiseMetrology

PS2-07

TSOM Fin-FET 구조 Bright Field / Dark Field Composite image 및 비율 최적화

김세정, 주지용, 이준성, *이준호 (Kongju Nationa Univ)

디스플레이에서 defect을 검출하기 위한 방식 중 하나로 사용할 수 있는 TSOM(Through-focus Scanning Optical Microscopy)은 In-focus 및 Defocus 데이터를 Z 축으로 스캐닝하여 정보를 도출한다. 또한 Bright-field 이미지와 Dark-field 이미지를 TSOM 이미지화 시켜 두 영역에 대한 데이터를 얻을 수 있다. 본 연구에서는 두 영역 데이터를 합성시켜 식별된 Taget의 정확성을 상향시킬 수 있음을 확인했으며, 나아가 불분명한 Taget을 특정할 수 있을 것으로 전망한다.

| Keywords : 계측 및 검사, TSOM

PS2-08

Defect Localization through Multi-Modal Deep Learning: Comparing Unaligned Camera and Blueprint Images

이상빈, 윤응구, *안태균 (세이지)

Defects such as shorts and scratches are easily identifiable in camera images. However, some defects, such as missing entire structures, may not be spotted due to the absence of distinctive visual features. In order to detect defects with deep learning models in these instances, comparing images with blueprints that incorporates the following steps is necessary: 1) Alignment of camera images and blueprints, as they are typically unaligned. 2) Localization of structural discrepancies between camera images and blueprints to inform the user of the decision rationale.Previous works often fall short in addressing these needs. Most alignment techniques fail when matching images from different domains. Additionally, existing inspection models, primarily based on deep learning, are designed to handle single-modality input. Although some multi-modal models exist, they frequently struggle to accurately localize discrepancies between the two modalities.To address these issues, we developed a novel multi-modal deep learning framework that first aligns camera images with unaligned blueprint images and then accurately classifies and localizes defect areas by comparing them. The proposed alignment and localization method can effectively handle two modalities, even from vastly different domains, such as rich color camera images and simple binarized blueprint images.

| Keywords : Defect Localization, Multi-Modal Alignment, Multi-Modal Comparison

PS2-09

TSOM의 암시야 적용 및 FinFET 선폭 계측 연구

이준성, 주지용, 김세정, *이준호 (Kongju Nationa Univ)

TSOM(Through focus Scanning Optical Microscopy)은 광학현미경과 같이, BF(Bright Field), DF(Dark Field) 방식이 존재한다. DF 기법은 반도체 공정에서 중요한 MI 기법으로 사용될 수 있다. 기존의 TSOM 기법은 직접 타깃에 비추는 BF 조명 방식을 이용하여 배경광에 의해 대비가 낮은 경향이 있다. 반면, DF 기법은 비축 조명으로 타깃을 조사하여 산란광이 검출기에 들어와 배경이 어둡기 때문에 대비가 높고, 따라서 타깃의 특정 부분이나 경계를 강조하는 장점이 있다. 이러한 특성을 이용하여 DF 기법은 반도체 디바이스의 미세한 패턴 및 결함을 검출하고 측정하는 데 매우 유용하다. 우리는 DF-TSOM의 실험적으로 비축 조명의 조사각도 최적화 및 TSOM Data의 MSD 분석을 통해 반도체 FinFET의 선폭 계측 연구를 진행하였다.

| Keywords : TSOM, Dark Field, Inspection, Metrology

PS2-10

Applicability of thermionic LaB6 virtualrnsource mode electron gun in electron beam lithography

이하림, 함영권, 오가와 타카시, *박인용 (KRISS)

Electron sources with higher brightness and narrower energy spreads open newrnavenues for creating fine patterns with high spatial resolution and increasedrnthroughput. Optimizing working conditions to enhance the performance of thernelectron source is crucial for next-generation electron beam lithography (EBL).rnIn this study, we propose a novel electron beam source mode utilizing Lanthanumrnhexaboride (LaB6), specifically the virtual source mode electronrngun, to explore its potential in EBL. Experimental results, which align wellrnwith simulations, demonstrate that the virtual source mode offers higher beam brightnessrnand narrower energy distribution compared to the commonly used crossover mode.rnIn virtual source mode, an energy distribution of 0.55 eV and a high angularrncurrent density of 33 mA/sr were measured, which are ideal for high-resolutionrnEBL. Typically, an electron source with low acceleration energy has lower brightness,rnand energy spread significantly affects spatial resolution. However, this newrnsource can overcome these limitations by optimizing the emitting conditions ofrnLaB6 even at 500 eV. This study showcases the exceptionalrnperformance of LaB6 electron sources and suggests their potential forrnbroader application in scientific and industrial fields, advancing EBL technology.

| Keywords : Lanthanum hexaboride, electron source, energyrndistribution, high angular current density, electron beam lithography, lowrnvoltage, virtual source mode

PS2-11

비선형 3차조화파 생성에서의 근적외선 구동빔 파면 변조를 통한 심자외선 빔 패턴의 능동 제어

원승재, 김정윤, 김태원 , 김병기 (TOKYOTECH), 최승만 , 김승우 , *김영진 (KAIST)

극자외선 (Extreme-ultraviolet)을 포함한 심자외선 (Deep-ultraviolet)rn이하 파장대역의 광원은 높은 광자 에너지와 우수한 공간분해능을 바탕으로 리소그래피, 트랜지스터 선폭 측정과 같은 다양한 반도체 공정 분야에서 각광받고 있다. 하지만, 심자외선 이하 파장은 대부분의 광학 물질에 높은 흡수 특성을 가지기 때문에, 빔의 집광이나 파면 제어를 위해서는 프레넬 존 플레이트 또는 다층박막 거울 등 복잡한 형태의 광학계가 요구된다. 본 논문에서는 비선형 조화파 현상을 기반으로 생성된 심자외선 광원의 빔 형태를 심자외선 광학계 없이 능동적으로 변조하는 기법을 제안한다. 공간 광 변조기 (Spatialrnlight modulator, SLM)로부터 파면이 변조된 근적외선 구동레이저 (파장 800 nm, 펄스폭 40rnfs, 반복률 1kHz)를 마그네슘 옥사이드 결정 (MgOrncrystal)에 입사시킴으로써, 생성된 3차 조화파 심자외선 (DUV,rn파장 266rnnm)의 빔 형태를 제어하였다. 고체매질에서의 비선형 조화파 생성 과정은 짧은 반응 길이로 인해 구동레이저의 시공간적 가간섭성이 유지되는 특성을 가지기 때문에, 구동레이저의 위상 또는 파면 정보를 조화파로 인계할 수 있다. 이러한 조화파 빔 제어를 통하여, 심자외선 기반 초고분해능 현미경법 (Super-resolution microscopy)을 위한 사인파 형태의 구조화빔을 생성하였고, 빔의 주기와 가시도를 측정하였다. 해당 기술을 향후 고차조화파 극자외선 대역으로 확장 시 극자외선 기반 구조화빔의 생성이 가능하다고 보여진다. 본 연구의 조화파 공간제어 기법은 심자외선 또는 극자외선 광원 기반의 정밀 패터닝 또는 초정밀 반도체 선폭 및 결함 측정 분야로의 효과적인 활용이 예상된다.

| Keywords : 심자외선, 빔 패턴 제어, 위상 변조기, 근적외선 구동레이저, 사인파 구조화빔

PS-2-12

ShapeMaster: Advanced 3D RCWA Modeling Software for Precision Optical Design and Analysis

성준제, 유신영, 이지원, 박서진 (Aurostechnology), 김광우, 김종정 (해도사)

Additionally, we verified ShapeMaster's Optical Critical Dimensions (OCD) inspection capability by correlating the OCD parameters from the reference data with those derived from the fitting results of the spectrum data sets. This validation process ensures the reliability of ShapeMaster's fitting algorithm, making it a powerful tool for optical design and analysis.

| Keywords : ShapeMaster, RCWA, FMM, OCD, 3D modeling, Metrology inspection, Aurostechnology, Haedosa

PS2-13

Novel EUV lighting sources with carbon nanotube based on cold cathode electron beam(C-beam) irradiation technique

김익수, 천수빈, 오소민, *박규창 (KYUNG HEE Univ)

In this paper, we investigate on the novel EUV lighting sources based on cold cathode electron beam irradiation technique. Conventional EUV lighting source based on LPP (laser produced plasma) or DPP (discharge produced plasma) has several problems with cost and debris. C-beam technology can provide solutions with these problems by its excellent property such as low energy distribution, high current density, narrow beam divergence angle. The EUV lighting source based on C-beam irradiation uses surface excitation of target materials rather than hot plasma. By using surface excitation, we can prevent the debris issue that can damage the optic and exposure system with low cost. In addition, we can control the intensity of EUV lighting source by adjust impact power of C-beam source efficiently. Furthermore, we can modify the EUV light's trajectory and intensity by adapting electron's optic without any loss of efficiency.We evaluate our EUV lighting source performance with photodiode equipped Zr filter to purify the EUV wavelength. Furthermore, we adapted EUV mirror and intermediate focus block for the accurate measurement. With this paper, we suggest EUV inspection tool based on cold cathode electron beam that can contribute to next generation high volume manufacturing in the semiconductor industry. Vertically aligned carbon nanotube (VACNT) can provide high quality EUV lighting source by its excellent characteristics as we mentioned. Moreover, based on this study, we will propose EUV lighting and lithography with different target materials based on C-beam technique that can conduct accurate patterning for the high specification semiconductor system for the next step of this study.

| Keywords : C-beam, Debris free, EUV inspection, surface excitation

PS-2-14

Development of cold cathode-based electron beam (C-beam) technology for scanning electron microscope imaging applications

RavindraPatil, Aniket Karande, Jung Hyun jin, *Kyu Chang Park (KYUNG HEE Univ)

This paper explores the development of cold cathode-based electron beam (C-Beam) technology for scanning electron microscope (SEM) imaging. Traditional SEM electron sources, such as thermionic and field emission sources, face issues like high energy consumption, thermal instability, and limited lifespan. C-beam technology addresses these challenges by using cold cathodes, which offer benefits such as reduced energy requirements, lower thermal emissions, and longer operational life.The development process includes optimizing cold cathode materials for efficient and stable electron emission, along with innovative design and control mechanisms to enhance electron beam performance. Initial tests demonstrate that C-beam technology provides higher resolution and improved imaging contrast compared to conventional sources, with lower operating temperatures that minimize thermal damage to samples. This makes C-beam technology ideal for imaging delicate materials such as biological specimens and nanoscale structures. This research highlights the potential of C-beam technology to significantly enhance SEM imaging capabilities, providing a more efficient and stable alternative. Moreover, the efficiency of the electron beam is crucial for electron microscopy's performance. Vertically aligned carbon nanotubes (VACNTs) offer a revolutionary alternative to traditional sources. Advanced growth methods produce brighter beams due to their sharp tips and efficient field emission, enhancing contrast and signal-to-noise ratios. Stable diode and triode current is essential for maintaining beam focus and intensity, ensuring high-quality images. This study underscores the importance of emission current, stability, and resolution, with simulation results showcasing the potential of VACNTs in improving electron microscopy.

| Keywords : Electronrnsource, Cold cathode, Field emission, Electron emission

PS2-15

Non-destructive measurement of semiconductorrnelectrical properties using tera-hertz-based in-line equipment technology

김원태, *양유신 (삼성전자 반도체연구소)

Terahertz (THz) technologyrnhas been anticipated to be a potential method that can measure the sheetrnresistance in the cell area, due to its high signal contrast by interactionrnwith free carriers in conducting thin films. However, in semiconductorrnmanufacturing, if base-doped silicon wafers used as a substrate have slightrndoping differences or gradients, it becomes difficult to measure the sheetrnresistance of the thin film. Typically, to solve this issue, transmissionrnsignals are measured before the process for reference. This double-measurementrnprocess negatively affects productivity. In this study,rnwe propose the world's first in-line THz based equipment technology forrnnon-destructive measurement of semiconductor electrical properties of thinrnfilms and surfaces on unknown substrates. The multiple echoes in a single THzrntransient obtained using a vertically aligned photoconductive antenna in arntransmission setup were analyzed to extract the transmission and reflectionrnproperties of thin films. We measured the in-cell resistance of semiconductorrnproducts in the production line, and the calculated values showed a highrncorrelation (R^2 ~0.97) with the electrical characteristics of the thin film ofrnthe DRAM. This demonstrates the potential of THz technology in semiconductorrnmanufacturing, even without prior knowledge of THz optical properties of thernsubstrates.

| Keywords : Terahertz, In-line equipment technology, Semiconductor, Sheet resistance, Thinrnfilm

PS-2-16

Advanced non-destructive imaging for super-resolution wafer inspection of highly periodic structures

이호준, 김형진, 신준호, 진영욱, 김진용, 김옥래, *이명준 (SAMSUNG)

The increasing complexity of semiconductor processes has led to a growing demand for high-reolution, large-area imaging systems for non-destructive wafer inspection. Recent attempts have been made to overcome the challenge of simultaneously achieving high-resolution and a wide field of view (FOV) using computational imaging techniques. Computational imaging recovers the complete electrical field of both the object and probe without prior knowledge by scanning with overlapping illumination, ensuring that each part of the object is illuminated multiple times. However, in imaging of highly periodic structures like DRAM and VNAND, scanning the illumination position results in minimal variations in the measured optical information due to the symmetry of the structure. Here, we presents an innovative approach using a reflection-type imaging system combined with a spatial light modulator (SLM) to program the illumination pattern, thereby expanding the applicability of inspection to both periodic and non-periodic structures in wafer manufacturing. This novel system brings about significant improvements, increasing the accuracy of periodic pattern image reconstruction from 59.8 % to 98.5 %. Furthermore, by substituting physical wafer position scanning with optical illumination pattern scanning using a SLM, the system reduces scanning position error from 266 nm to 47 nm in the scanning imaging modality.

| Keywords : Computational imaging, Wafer inspection, High-resolution imaging

PS-2-17

3D Thermal Property Imaging System with Frequency-Domain Thermoreflectance

김지현, 서동윤, 한규성, *조정완 (성균관대)

Pump-probe thermoreflectance techniques,rnincluding frequency-domain thermoreflectance (FDTR) and time-domainrn-thermoreflectance (TDTR), have garnered significant attention due to theirrnability to measure thermal properties at micro/nano scales. The probing depthrnof thermoreflectance techniques is determined by the thermal penetration depthrnof the laser, which is a function of frequency. In particular, FDTR is morernsensitive to deeper regions below the surface compared to otherrnthermoreflectance techniques due to its frequency domain characteristics. Inrnthis work, we developed a 3D thermal property imaging system using FDTR. Byrnintegrating a motorized stage, we expanded the FDTR system to achieve 2D (XY) rnthermal property imaging. For depth (Z) probing, we controlled the probingrndepth by adjusting the frequency. To demonstrate our 3D thermal propertyrnimaging system, we imaged the 3D thermal properties of a 380 nm Ga2O3rnheteroepitaxial thin film grown on Al2O3 by MOCVD. This system can be appliedrnto assess bonding and film quality.rnrn

| Keywords : Thermal conductivity, Thermal boundary resistance, Thermal boundary conductance, Thermoreflectance

PS3-01

실크 단백질에 기반한 마이크로 컬러필터

이지현, 남관현, 최주완, *김성환 (Hanyang Univ)

강한 속박에 의해 빛을 제어하는 광학 공진기는 빛과 물질 사이의 상호작용을 극대화할 수 있어 고품위 센싱과 이미징을 가능하게 한다. 그중 패브리-페롯 에탈론에 기반한 금속-절연체-금속 (metal-insulator-metal, MIM) 공진기는 고품위 공진 모드를 상대적으로 간단한 구조로 구현할 수 있어 많은 관심을 받고 있다. 여기에 천연 실크 단백질은 기존 MIM에서 활용된 절연체와 달리 생체 적합성이 우수하고, 수분에 민감하여 바이오 응용에 적합하다. 그러나 이 필터를 미세 패턴화하는 것은 아직 도전적인 과제이다. 본 연구에서는 in-lab 포토리소그래피를 통해 미세 패턴화된 실크 기반 컬러필터의 제작과 그 응용에 대해 보고한다. 구현한 컬러필터는 수중 환경 및 용액의 농도에 따라 발생하는 공진 파장 변조를 독립 픽셀 디스플레이를 통해 시각적으로 제공했다. 실크 기반 컬러필터 소자는 향후 화학 물질에 취약한 바이오 물질 및 식품에 적용 가능한 생체 친화적 광 디바이스로 활용이 가능할 것이다.

| Keywords : 실크 단백질, 포토리소그래피, 센싱, 금속-절연체-금속 공진기(metal-insulator-metal resonator), 컬러필터

PS3-02

Development of a micro/nano patterning process for high-curvature three-dimensional structures of various shapes

이성혁, *Hwan-Jin Jeon (TECH Univ)

Uniform patterns of micro-sized curved structures have played a key role in various fields such as micro ball lens arrays, anti-reflection films, display devices, biochip and lighting devices. Recently, many research groups are developing processes that can fabricate regular curved structure arrays in large areas. Among the technologies that can produce curved structural patterns, the technologies that have been most actively researched recently include colloid lithography, thermal reflow, and inkjet printing technologies. Thermal reflow methods struggle to control contact angles, while microdroplet jetting struggles to maintain uniform size and spacing. MEMS-based methods enable uniform production, but require expensive equipment and complex processes. To overcome these limitations, we developed an isolated air-pocket lithography (IAL) method that utilizes gas expansion to form high curvature patterns. Despite the initial difficulties in producing lenticular lenses with linear curved structures and fine nanometer-scale patterns, we devised a solution that minimizes pressure interference during gas expansion. Our method is simple, cost-effective, and does not require special equipment. This new approach shows promise for applications in electromechanical systems, biosensors, optical sensors, displays, and fluidic devices, providing a versatile and efficient technique for fabricating high-performance, stretchable, and conductive films.

| Keywords : high-curvature, IAL. linear, nano pattern, gas expansion

PS4-01

Synthesis and Characterizations of Non-Alkyl Tin Oxo Cluster CNU-TOC-01(4C-C) and its Application to EUV Inorganic Resist

윤혁, 방지영, 김민엽 CHONNAM National Univ), 문형배, 김철민 (포켐래버래토리), 노우시, 김기정 (POSTECH),
이희선, 허규용 (KRICT), *정현담 (CHONNAM National Univ)

We introduce a non-alkyl tin-oxo cluster, CNU-TOC-01(4C-C), synthesized through a reflux-based solution reaction using SnCl2, H2O, and pyrazole. Using field desorption time-of-flight mass spectrometry (FD-TOF MS) and small-angle X-ray scattering(SAXS), CNU-TOC-01(4C-C) is characterized as a cyclic cluster with a molecular formula Sn4Cl3(C3N2H4)(C3N2H3)H4O8. The cluster size was measured to be 11.6 Å by SAXS, and estimated to be 11.1 Å lengthwise in quantum chemical calculation. The synthesized material exhibits an extreme ultraviolet (EUV) linear absorption coefficient of 89 μm^{-1}, dramatically higher than those of conventional tin oxo clusters used in EUV lithography (EUVL). Initial application in EUVL and electron beam lithography (EBL) achieved fine line and space pattes with potential for ultra-fine resolutions upon optimization. CNU-TOC-01(4C-C)'s high etch resistance underscores its exceptional suitability as an advanced resist material for future lithographic applications.

| Keywords : Extreme Ultraviolet Lithography, Inorganic Resist, Metal Oxide Resist, Tin Oxo Cluster

PS4-02

Optimization of Process Conditions for Enhanced Patterning Performance of EUV Inorganic Resist CNU-TOC-01(4C-C)

윤혁, 백승용, 정현담 (CHONNAM National Univ)

The EUV resist CNU-TOC-01(4C-C) demonstrates patterning capabilities on thermally oxidized silicon (SiO_2) substrate. However, it encounters issues when applied on spin-on carbon (SOC) layers, likely due to minimal interfacial reactions between SOC and CNU-TOC-01(4C-C). To address this, a spin-on glass (SOG) type underlayer (UL) material was developed by copolymerizing TEOS ($Si(OEt)_4$) and MTMS ($SiMe(OMe)_3$). Coating the SOG on SOC, followed by the application of CNU-TOC-01(4C-C), enabled effective patterning of the resist. CNU-TOC-01(4C-C) exhibits a high EUV absorption coefficient of 82 μm^{-1}. As a result, only about 7% of the EUV photons penetrate through a 30 nm thick CNU-TOC-01(4C-C) film to the UL interface, which would be not sufficient to proceed interfacial reactions. By reducing the resist film thickness from 30 nm to 18 nm, the sensitivity of CNU-TOC-01(4C-C) improved significantly (D_{50} = 225 $\mu C/cm^2$ to 66 $\mu C/cm^2$). Applying the standard post apply bake (PAB) condition of 180°C for 3 min to the CNU-TOC-01(4C-C) film and analyzing with XPS revealed increased condensation of Sn-OH to Sn-O-Sn compared to films baked at 100°C for 3 min. Adjusting the PAB and PEB temperatures to 100°C and using butyl acetate as the developer reduced Sn-OH condensation in unexposed areas, enabling patterning. However, this approach compromised film vacuum stability, even necessitating further solutions. Before hard baking, inspections showed line and space patterns with noticeable waviness. Post hard baking at 250°C for 3 min, inspections indicated significant reduction in pattern waviness, suggesting improved line edge roughness. This study presents optimized process conditions to enhance the patterning performance of the EUV resist CNU-TOC-01(4C-C), addressing critical challenges and achieving better resolution and stability.

| Keywords : EUV lithography, inorganic resist, underlayer, process optimization

PS4-03

실크 단백질 내 2.5D 미세패턴화 된 암호화 정보의 전자빔 리소그래피 전사

최주완 (Hanyang Univ), 이태윤, 전헌수 (Seoul National Univ), *김성환 (Hanyang Univ)

나노패턴을 생체소재에 접목시키는 기술은 생체적합성을 지닌 의공학 소자 개발에 있어 불가결한 요소이다. 나노패터닝 기술 중 전자빔 리소그래피는 실크 단백질에 적용하여 고해상도의 나노구조를 구현하는 것이 가능하다. 그러나 고에너지 전자의 주입은 실크 생체재료 내 기능성 물질의 성능을 저하시킬 우려가 있다. 이러한 문제점을 극복하기 위해 저에너지 전자빔을 활용, 노광 후 가교결합을 유도하는 방식으로 실크 위 나노패터닝을 수행한 결과를 보고한다. 본 방식을 통해 실크 단백질에 2D 및 2.5D 패턴 구조를 근접효과 없이 고해상도로 집적하는 것이 가능했으며, 실크의 분자구조 변화를 활용해 암호화 된 보안 코드 생성 응용도 가능하였다. 이 제작 공정을 더 발전시킨다면 향후 다양한 의공학용 광학, 전자소자 제작을 위해 활용될 수 있을 것이다.

| Keywords : 실크 단백질, 전자빔 리소그래피,2.5D 패턴, 보안코드, 의공학용 소자

PS4-04

Synthesis and Characterization of 4-Amino Benzoate Zinc Oxo Cluster for EUV Inorganic Resist

이가현, *정현담 (CHONNAM National Univ)

Zincrnoxo clusters (ZOCs), which exhibit higher EUV absorption cross-sections compared to ChemicallyrnAmplified Resist(-CAR), are being recognized as potential EUV photoresistrnmaterials due to their high EUV sensitivity. Additionally, their small-rnmolecular size can offer high resolution. As inorganic photoresist materials,rnZOCs possess excellent dry etch resistance and excellent mechanical properties.rnCarboxylates are commonly used as ligands in EUV photoresists as they undergorndecar-boxylation upon EUV exposure A recent study[1]rnsuggests that phenylrngroups at the cluster termini can enhance the thermal stability of ZOCs, due tornthe electron-rich and rigid nature of aromatic rings, indicating the potentialrnfor incorporating aromatic ligands. Moreover, hydrogenrnbonding is anticipated to improve EUV performance by providing tight binding,rnre-ducing intermolecular spacing, and mitigating the spread of secondaryrnelectrons. Based on this, we decided to use 4-amino benzoic acid, whichrnfeatures an aromatic ring and the ability to form hydrogen bonds, as a ligandrnfor ZOCs. The ligand of trifluoroacetate ZOC was exchanged with 4-amino benzoicrnacid, and the synthesized material was analyzed using NMR and MALDI-TOF. Tornevaluate the photoresist performance of 4-aminobenzoate zinc oxo cluster (ZOC_4ABA),rnit was dissolved in ethyl lactate and spin-coated onto a Si wafer. It was thenrnsubjected to electron beam lithography, which confirmed an electron beamrnsensitivity (D50) of 107 μC/cm². However, EUV lithography performedrnat Lawrence Berkeley National Laboratory(LBNL) did not succeed in obtainingrnfine patterns.

| Keywords : zinc oxo cluster, EUV inorganic photoresist,

PS4-05

Synthesis and Characterization of Siloxane Core-Arm Type Molecular Resist for EUV Lithography

백승용, 윤혁, *정현담 (CHONNAM National Univ)

This study aims to introduce the tert-butyloxycarbonyl (tBOC) structure, which is widely used as an acid-labile group, into the siloxane core and to investigate the properties exhibited by the tBOC structure in siloxane resists. TS-T4(tBOC)4 was synthesized by introducing di-tert-butyl dicarbonate to tetrahydroxy-tetramethyl-cyclotetrasiloxane using dimethylaminopyridine (DMAP) as a catalyst. The molecular structure of the synthesized material was confirmed by proton nuclear magnetic resonance spectroscopy (1H-NMR), and its lithographic properties were characterized through electron-beam lithography (EBL). The remaining thicknesses of the patterns were measured using an atomic force microscopy (AFM). As a result, it was confirmed that TS-T4(tBOC)4 has ultra-high sensitivity (D50 = 1.5 μC/cm2) but low contrast (γ = 0.8). Additionally, to address the issue of excessive sensitivity, a trimethoxysilane structure was introduced into the core to suppress sensitivity. In conclusion, we identified a slightly lower sensitivity (D50 = 4.6 μC/cm2) and contrast (γ = 0.9), and although the lithographic properties were confirmed using EUVL, it showed overdose due to the still high sensitivity.

| Keywords :Molecular Resist, EUV lithography, siloxane core, sensitivity, contrast

PS4-06

The Investigation of the Effect of Electron Beam Irradiation on Dibenzyltin Diacetate Thin Film Using Local Analysis and Quantum Chemical Calculations

윤현성, 윤혁, 정현담 (CHONNAM National Univ)

This study investigates the impact of extreme ultraviolet (EUV) light on the chemical alteration of photoresists (PRs), termed EUV-induced material alteration (EUV-MA). EUV-MA plays a pivotal role in photolithography, affecting the manifestation of chemical contrast in PR upon exposure and its subsequent enhancement during development. To estimate the EUV-MA of a PR, one must investigate the changes in the molecular structure of the PR before and after exposure to EUV. However, the limited accessibility of EUV light sources is a constraint in the study. To circumvent this, we utilized electron beam (E-Beam) instead of EUV, based on the similarity in energy distribution of secondary electrons generated by both sources. Our examination focused on the response of dibenzyltin diacetate thin films to E-Beam irradiation, using localized analysis methods such as Fourier-transform infrared spectroscopy (FT-IR) and time-of-flight secondary ion mass spectrometry (TOF-SIMS). Our findings reveal that not only the benzyl group but also the acetate group in dibenzyltin diacetate molecules can dissociate. However, it was unclear whether the dissociation of the acetate group involved the breaking of the tin-oxygen bond or the oxygen-carbon bond within the acetate. To clarify this, we employed the quantum chemistry calculation program Quantemol Electron Collision. Due to limitations of the program, we used dimethyltin diacetate instead of dibenzyltin diacetate and calculated the cross-sections of both bonds using the R-matrix method. To directly compute the dibenzyltin diacetate molecule, we developed a method to estimate the cross-sections for neutral dissociation and dissociative electron attachment by calculating the inner product of the molecular orbitals involved as the molecule excites to various states and the natural bond orbitals within the molecule, instead of using the R-matrix method.

| Keywords : E-beam lithography, energy distribution of secondary electron, dibenzyltin diacetate, neutral dissociation, dissociative electron attachment

PS4-07

Vacuum-deposited Fluorinated Photoresist Formulationsrnfor OLED Pixel Formation

김가영, 최효은, 권유정, 김명웅, *이진균 (Inha Univ), 장귀원, 김태우, 팽기욱 (SUNGKYUNKWAN Univ), 소은영, 김두홍, 정병준 (University of Seoul)

포토리소그래피rn공정을 이용하여 유기전계발광 다이오드(OLED)의 화소를 형성하고자 할 때 유기 반도체 박막을 증착한rn후 기판을 증착 챔버 밖으로 꺼내어 용액 코팅 공정을 진행해야 한다. 하지만 OLED는 대기 중 수분 및 산소와 접촉하면 성능이 급격히 저하되는 문제가 있다. 본 연구에서 이러한 문제를 해결하기 위해, 진공 조건하에서 증착된 OLED 박막이 대기 조건에 노출되기 전에 동일한 환경에서 OLED 박막rn상부에 증착될 수 있는 불소화 포토레지스트 조성물을 개발하였다. 해당 조성물로 증착된 박막은 조성물의rn비율과 구성 상태에 따라 포지티브형 또는 네가티브형 패턴을 형성할 수 있었다. 패턴화된 박막의 건식각rn또는 리프트오프 공정을 진행한 후 최종적으로 포토레지스트 박막을 제거하면 패턴화된 유기 반도체 박막을 얻을 수 있음을 확인하였다. 이 조성물은 스텐실 형성뿐만 아니라, 물리적, 화학적 침해조건에 취약한 OLED 박막에 대한 보호층 역할을 수행할rn수 있어 소자 성능 저하를 최소화하는데 유리할 것으로 기대된다.

| Keywords : Photolithography, OLED, Vacuum-deposited, Fluorinated Photoresist Formulations

PS4-08

Etchant-Free Thermal Developable Extreme Ultraviolet Photoresist Utilizing N-Heterocyclic Carbene-Metal Ligand Structures

김도원, 김상진, 문인욱, *홍석원 (GIST)

Extreme ultraviolet (EUV) lithography is crucial for advancing semiconductor technology by significantly reducing device dimensions and sustaining Moore's Law. Traditional wet processing methods limit EUV lithography's potential, necessitating the development of dry development technology to overcome environmental and performance constraints. We introduce an etchant-free, dry-developable EUV photoresist made of small molecules with N-heterocyclic carbene (NHC) metal-ligand complexes. Our photoresists show exceptional EUV sensitivity, achieving half-saturation at 8.5 or 27 mJ/cm^2. They feature a thermal treatment for removing unexposed photoresist areas, termed thermal development. This material achieves a 40 nm half-pitch resolution via wet development and a 90 nm resolution via thermal development, showcasing its potential for high-resolution patterning and dry-developed nanopatterns.

| Keywords :extreme ultraviolet, dry development technique,rnmetal-organic photoresists

PS-4-9

Enhancing Sensitivity of Inorganic Resists for EUV Lithography through Metal Sensitizers

방지영, 윤혁, 기원철 (CHONNAM National Univ), 노시우, 김기정(POSTECH), *정현담 (CHONNAM National Univ)

While advancements in EUV equipment, including High-NA and Hyper-NA tools, have been rapid, progress in photoresist development remains insufficient. Inorganic photoresists are anticipated as next-generation resists due to their high mechanical strength and dry etching resistance. In our previous study, we used tetrahydroxytetramethylcyclotetrasiloxane as an EUV resist. Although it initially achieved 22 nm HP L/S patterns in EUVL, repeated experiments showed decreased EUV absorbance, resulting in the failure to form L/S patterns. To address this, we added metals with a high EUV absorption cross-section as sensitizers to improve sensitivity. Tin oxo cluster CNU-TOC-01 (4C-C) and zinc oxo cluster Zn4O(COOCF3)6 were mixed into the solution as sensitizers, respectively, and we compared the electron beam sensitivity. The metal sensitizers appear to enhance sensitivity by acting as catalysts for the polycondensation reaction in addition to generating secondary electrons